RF Energy Harvester with Peak Power Conversion Efficiency Tracking

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***Abstract*—Rectifier circuits or power harvesters are a critical module in a variety of wireless sensors, radio frequency identification (RFID) tags, and Internet-of-Thing (IoT) devices relying on harvested power from radio waves. The threshold compensation circuit techniques have been proposed in the literature to improve the Power Conversion Efficiency (PCE) of CMOS-based rectifiers. However, these circuits are designed to achieve maximum PCE at a specific input power level, and has significantly lower efficiency at other input power levels. In this paper, we propose a novel energy harvester which maximises its PCE over a wide input power range. The proposed design relies on sensing of the rectifier output voltage, management of the output current and reconfiguration of the rectifier. The design, which operates at 915 MHz, is demonstrated through simulations in a 130 nm CMOS process. The simulation results show that the harvester manages to develop a 3 V DC with -25 dBm input power sensitivity and its PCE remains above 60% for 23 dB input power range.**

I. Introduction

In recent years, with the emerging interest in IoT (Internet of Things), there is an increasing focus on energy harvesting circuits. One very popular branch of these works is energy harvesting from the surrounding EM (electromagnetic) waves. In particular, RF harvesting in the UHF band has been given substantial attention, as a longer power transfer distance can be achieved. As such, recitifers, as the core of the harvester, has been designed to be efficient at minimum input power, because high sensitivity and long operation range are desired.

Small input power to the rectifier, for a given antenna rectifier interface, means a small input voltage amplitude across the rectifier. When this amplitude becomes so small that it is below the threshold of the transistors used in the rectifier, the rectifier will be unable to convert the input AC to DC. Threshold-compensated rectifiers have been demonstrated as the definitive circuit approach to the design of highly sensitive and low-cost CMOS-based rectifiers, and more than a decade of effort has been invested in perfecting this circuit approach [1]–[5] and [6]. However, with most of the existing rectifier designs, their power conversion efficiency (PCE) only peaks at a particular input power and can be substantially worse at other input power levels. Hence, these power harvesting rectifiers are unable to maintain the peak PCE over a wide range of input powers to maximize on available incident energy.

In the context of fully-passive RFID tag, the main concern for the design of rectifiers is sensitivity. However, this has been changed with the proposal of hybrid-powered RFID tag [7]. In a hybrid tag, the excess energy is stored in a capacitor or a rechargable battery when the tag is close to the reader antenna. The stored energy can then be used when the tag is moving awary from the reader where the harvested power is insufficent to supply the tag circuitry. Because the excess power can be stored for later use, it is no longer sufficient to be efficient just at minimum input power as high efficiency is desired at all input power levels.

Notably, maximum power efficiency tracking was explored in [8]–[10]. [8] requires an external microcontroller and [9] operates with milliwatt-level input power, thus both of them are unsuitable for ultra-low power energy harvestering. In [10], the rectifier is designed to operate at 50 kHz, thus it is ill-suited to energy harvesting in the UHF band.

In this paper, we propose a UHF energy harvester that achieves excellent PCE across a wide input power range while maintaining competitive sensitivity. Our proposed design is unique in that it tracks the maximum power efficiency by exploiting the relationship between the output voltage and the PCE resulting in an efficient and compact solution. We start by describing the limitation of threshold-compensated rectifier in Section II. Then we describe the proposed peak PCE tracking technique in Section III. Proposed design and simulation results are presented in Section IV. Finally, conclusions will be drawn in Section V, followed by acknowledgement.

II. Limitation in Existing Threshold Compensated Rectifiers

Previous studies such as [2] and [4] have demonstrated the tight trade-off between forward passing and reverse leakage, preventing the rectifier from achieving high PCE over a wide range of input power. For most threshold-compensated rectifiers, the PCE is insignificant at very low input power, this is because the input power is too small to turn on the diode devices within the rectifier. Due to threshold compensation, diode devices within the rectifier turns on at relatively small input power. Thus, initially, as the input power increases, the forward passing capability of the diodes improve and subsequently the PCE of the rectifier improves. However, as the input power increases, the output voltage also increases; as the output voltage builds up and the threshold compensation is still being applied, the reverse leakage becomes significant and starts to dominate over the forward passing and, subsequently, the PCE starts to decrease. Therefore, the PCE peaks when the forward passing is balanced out by the reverse leakage, as shown in Figure 1.

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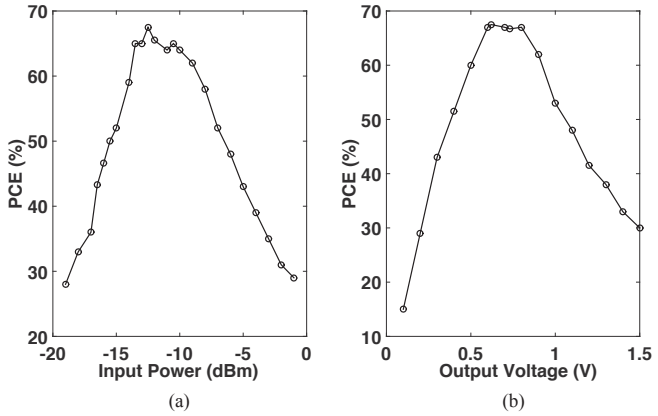


(a) (b)

Fig. 1. Peaking behavior in (a) input power vs PCE and (b) output voltage vs PCE, reproduced from the single stage differential-drive rectifier proposed in [4].

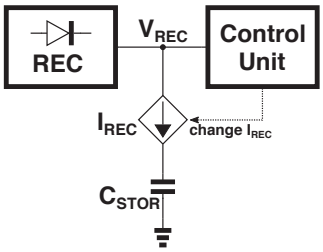


Fig. 2. A conceptual diagram of the proposed design, where the control unit regulates the output voltage of the rectifier $\mathrm{V_{REC}}$ by changing the output current of the rectifier $\mathrm{I_{REC}}$.

III. Peak PCE Tracking Technique

From Figure 1, we observe that if the output is regulated to the voltage where maximum PCE is achieved, the PCE can be optimized over a wide range of input power. One way to regulate the output voltage is to drain the output current while the input power increases. This increase in input power and subsequently an increase in the output voltage is counter-reacted by an increase in the drained current. Similarly, if the input power is decreased, the current drained from the output of the rectifier will be decreased, maintaining the output voltage at the pre-set voltage. This concept is illustrated in Figure 2.

To verify this, a 130 nm CMOS process was used for the following simulations and the simulation set-up is shown in Figure 3. The rectifier circuit topology used in Figure 3 is a 3-stage differential-drive CMOS rectifier [4], which is shown in Figure 4. In these simulations, the input power is swept from 10 μW up to 800 μW, while the current drawn from the rectifier output was set to 5 μA, 10 μA, 20 μA, 50 μA, 70 μA, 100 μA, 120 μA, and 150 μA at an operating frequency of 915 MHz. The simulated PCE as a function of input power and current is shown in Figure 5(a). In addition, the relationship between the output voltage and the PCE is plotted in Figure 5(b). Interestingly, as can be observed in Figure 5(b), the relationship between the output voltage and PCE shifts to a higher voltage as the output current increases and to a lower voltage as the output current decreases. Consequently, the PCE optimal voltage is a function of the output current.

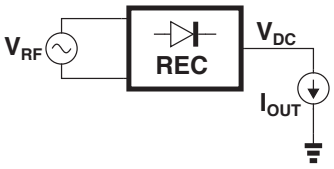


Fig. 3. The simulation set-up used to generate the simulation results shown in Figs. 5(a) & 5(b).

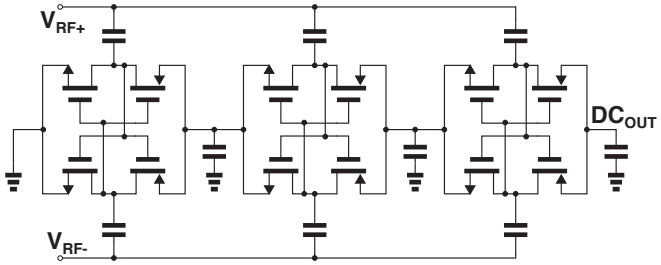
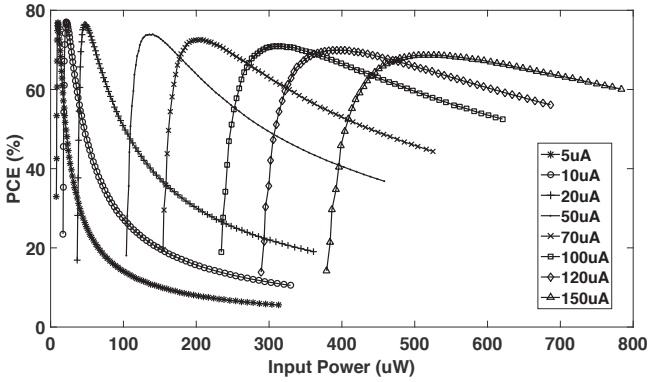


Fig. 4. The 3-stage differential-drive rectifier schematic.

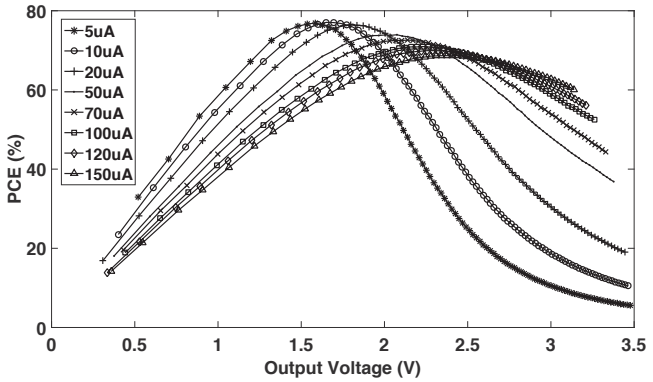
As the output voltage is regulated by changing the current drained from the output of the rectifier, the input power to the rectifier determines the output current and subsequently the PCE optimal voltage. Specifically, as input power increases, PCE optimal output voltage increases and output voltage vs PCE curves shifts to a higher voltage, and vice versa. Hence, as the input power changes, the optimal PCE cannot be achieved with the output regulated to a specific voltage.

However, it can be observed in Figure 5(b), as the output current varies by 30 times, the PCE optimal output voltage only varies by less than 2 times and good PCE is still achievable with slight deviation from the PCE optimal voltage. Thus, excellent PCE can be achieved over a reasonably wide input power range by just maintaining the output voltage at the optimal PCE voltage for the lowest current (i.e. 5 μA).

To further improve the input power dynamic range of the PCE, as the input power increases, the number of stages of the rectifier has to be reduced. As discussed previously, the output voltage vs PCE relationship is dictated by the charateristics of the individual rectifier stage. Since all stages are placed in series, the PCE optimal output voltage of all stages is simply the sum of the PCE optimal output voltage of each individual stage. When the number of stages reduces, the PCE optimal voltage for all stages decreases. Effectively, the overall output voltage vs PCE curve shifts to a lower voltage. This counter-reacts the output voltage vs PCE curve shifting to a higher voltage due to the increased input power. Similarly, as the input power decreases, the number of stages of the rectifier has to be increased. Increasing the number of stages of the rectifier shifts the output voltage vs PCE curve to a higher voltage, thus counter-reacting the curve shifting to a lower voltage due to the decreased input power. In summary, by properly reconfiguring the number of the stages of the rectifier as a function of the input power level, the PCE vs output voltage curve stays unshifted. Hence, the optimal PCE can be obtained at the same voltage, irrespective of the input power. The curve shifting process is illustrated in Figure 6 and the conceptual diagram of the improved design is illustrated in Figure 7.



(a)



(b)

Fig. 5. (a) Input power vs PCE and (b) output voltage vs PCE of the simulated 3-stage differential-drive rectifier.

Another merit of the proposed design is the prevention of dynamic reverse leakage. This is not to be confused with the reverse leakage discussed previously, which occurs in steady state. In systems where the rectifier is directly connected to the storage capacitor, in the event of a drop in input power, the charge already stored on the capacitor will potentially flow out of the capacitor and back into the rectifier. A classical solution to this problem is to design the last stage of the rectifier with diode-connected transistors [2] at the expense of lower power efficiency and sensitivity. In this design, as shown in Figure 7, the storage capacitor is shielded from the rectifier by a variable current source. When the input power drops, the control unit reduces I_{REC} so that V_{REC} stays at the pre-set voltage. With this approach, the reverse leakage is avoided without sacrificing the overall power efficiency or sensitivity.

IV. Proposed Reconfigurable Rectifier and Simulation Results

The circuit realization of the proposed fully-integrated energy harvester is illustrated in Figure 8. The control unit consists of comparator $COMP_1$, power MOSFET MP_{PWR} and diode-connected PMOS MP_{STR1} through to MP_{STRX}, which regulates the output voltage V_{REC} at 3 V; it also consists of PMOS transistor MP_{SN}, resistor R_{SN}, comparator $COMP_2$, inverters INV_1, INV_2 and MOS switches MP_{S1}, MN_{S1}, MP_{S2} and MP_{S3}, which reconfigures the number of stages of the

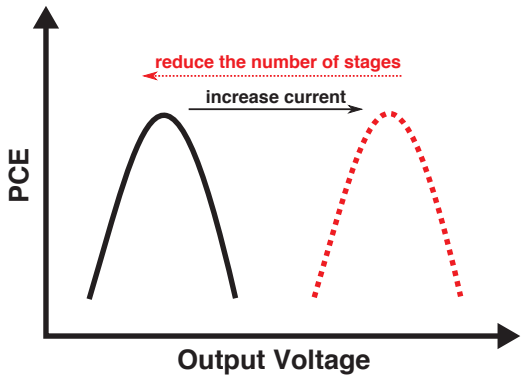


Fig. 6. Illustration of the curve shifting.

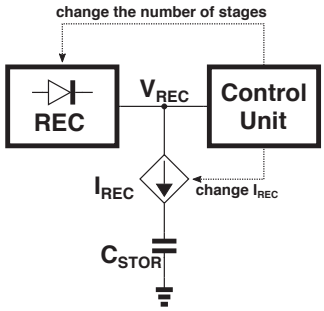


Fig. 7. Conceptual model of the improved design, where the control unit regulates the output voltage of the rectifier V_{REC} by changing the output current of the rectifier I_{REC} and it also reconfigures the number of stages within the rectifier as a function of input power.

rectifier. In addition, the 4-stage and 2-stage rectifier consists of the same differential-drive rectifier circuit as shown in Figure 4. To optimize the overall power efficiency and sensitivity, circuits within the control unit, including comparators and inverters, are designed to operate in deep subthreshold region so that their power consumption is minimized.

The operation principle is as follows: $COMP_1$, MP_{PWR} and the voltage divider realized by a string of diode-connected PMOS transistors regulates the V_{REC} at 3 V by changing

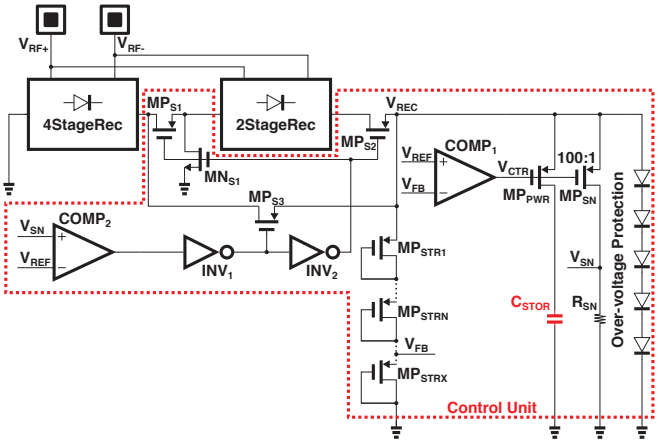


Fig. 8. Circuit realization of the proposed energy harvester.

TABLE I. PERFORMANCE COMPARISON

Design	Input Power Sensitivity	Peak Efficiency	Wideband Efficiency	Note
This Work	-25 dBm @3V (Capacitive Load)	70% @ -16 dBm	Above 60% over 23 dB input power range	Fully-integrated
[11]	-17 dBm @2V (Capacitive Load)	60% @ -3 dBm	Above 40% over 14 dB input power range	Fully-integrated
[12]	-27 dBm @1V (Capacitive Load)	40% @ -17 dBm	N/A	External microcontroller for optimization
[13]	-24 dBm @1.2V (10MΩ Load)	68% for the integrated boost converter	N/A	External inductor for boost converter

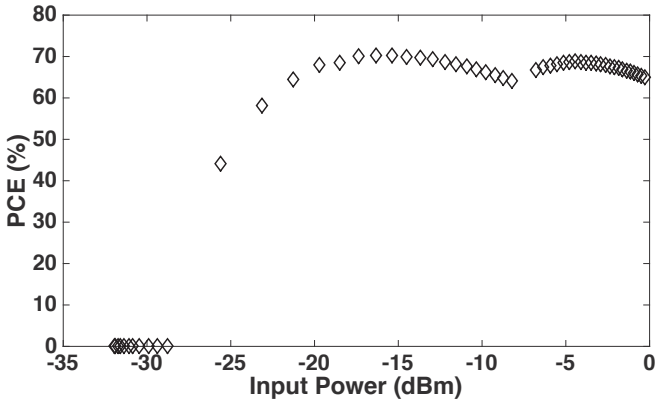


Fig. 9. Input Power vs PCE of the proposed design.

the current drained from the output of the rectifier through $\mathrm{MP_{PWR}}$ and all the current is directed into the capacitor $\mathrm{C_{STOR}}$ for storage. The width of $\mathrm{MP_{SN}}$ is 1/100 of $\mathrm{MP_{PWR}}$, thus it takes a tiny slice of the current through $\mathrm{MP_{PWR}}$ and passes it through the resistor $\mathrm{R_{SN}}$. When the output current increases, $\mathrm{V_{SN}}$ rises and when it becomes greater than $\mathrm{V_{REF}}$, $\mathrm{COMP_2}$ pulls up its output and the inverters and the MOS switches in Figure 8 reconfigures the rectifier from 6-stage to 4-stage.

The simulated PCE vs input power of the proposed harvester design is shown in Figure 9 and the simulation is conducted at 915 MHz. The PCE can be calculated as [4],

$$\mathrm{PCE} = \frac{\mathrm{P_{OUT}}}{\mathrm{P_{IN}}} \tag{1}$$

where $\mathrm{P_{IN}}$ and $\mathrm{P_{OUT}}$ are the measured input and output power after the system reaches steady state. There isn't a large number of designs which attempt to maintain high PCE across a wide input power range, as the motivation for this was not clear until the hybrid power concept [7]. A prior-art design [11] which also attempts to achieve high PCE over a wide input power range and two other start-of-the-art designs [12], [13] are included in Table I.

V. CONCLUSION

This paper proposed a novel UHF energy harvester with peak PCE tracking over a wide input power range. Our proposed design tracks the maximum PCE of threshold-compensated rectifiers through intellingently managing its output current and reconfiguration of the rectifier. Another contribution of this work is the prevention of reverse leakage without compromising the overall power efficiency and sensitivity of the energy harvester.

It is worth noting that this work focuses on the conversion efficiency. To ultimately optimize the overall system efficiency, matching technique has to be developed to minimise the mismatch between the varying input impedance of the rectifier and the impedance of the antenna. However, this aspect is beyond the scope of this paper and it will be investigated in another study.

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