Antennas, Waves, and Circuits in Radio Frequency Identification

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Doctor of Philosophy

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“All truths are easy to understand once they are discovered
– the point is to discover them.”

Galileo Galilei (1564-1642).
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High-performance electronic labelling systems require the separate components to be designed in an optimum way and with a consideration of their interactions with other components in the system. As with many system designs many aspects of the electrical and electronic discipline must be pursued with skill for a successful design to emerge. In addition to dealing with these matters, the author considers low cost and long range along with manufacturability as key criteria for a high-performance labelling system and thus has kept these aspects in mind throughout the component design process.

The first part of the work describes the design of both near-field and far-field UHF antennas including a UHF antenna which is combined with an HF antenna. In a second part of the work are investigations of techniques for reading UHF tags on a metal surface and HF tags inside a hole formed in metal. Finally, the designs of low-power and low-cost microelectronic circuits for passive tags are discussed. Each system element designed by the author has been fabricated for successful empirical evaluation.
Statement of Originality

Name: ___________________________  Program: ___________________________

This work contains no material which has been accepted for the award of any other degree or diploma in any university or other tertiary institution to David M. Hall and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text.

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Signature: ___________________________  Date: ___________________________
Acknowledgments

The author would like to thank his supervisor Professor Peter H. Cole for his tireless support in the study for and writing of this thesis. Professor Cole has provided the author with insights into RFID unequalled in this field of study. He has also provided funds for fabrications and sustenance during many a long night in the laboratory.

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Damith Ranasinghe for help with MATLAB.
Conventions

This thesis was typeset using the \LaTeXe\ software.

Australian English spelling is adopted.

Plain style is used for the author’s publications.

Harvard style is used for citation in this thesis.

SI units are used for physical units.

In schematics, transistor widths and lengths listed next to MOSFET symbols are in the order:

width
length
Publications of the Author


[18] Hall, David Malcolm; Pellet, Fabien; Tran, Tu, “Point of sale reading structure”, Australian Patent Application 2006902193
[34] Hall, David Malcolm; Cole, Peter Harold, “A system and method for interrogating electronic labels”, Australian Patent Application 2002216836
# Abbreviations

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<td>ABS</td>
<td>acrylonitrile butadiene styrene</td>
</tr>
<tr>
<td>AC</td>
<td>alternating current</td>
</tr>
<tr>
<td>Al</td>
<td>aluminium</td>
</tr>
<tr>
<td>ALOHA</td>
<td>an intermittent tag reply scheme</td>
</tr>
<tr>
<td>AM</td>
<td>amplitude modulation</td>
</tr>
<tr>
<td>AMI</td>
<td>American Microsystems Inc.</td>
</tr>
<tr>
<td>B</td>
<td>base</td>
</tr>
<tr>
<td>BNC</td>
<td>bayonet NeillConcelman</td>
</tr>
<tr>
<td>BW</td>
<td>bandwidth</td>
</tr>
<tr>
<td>C</td>
<td>capacitor or collector</td>
</tr>
<tr>
<td>CARP</td>
<td>carbon-amide reinforced plastic</td>
</tr>
<tr>
<td>CD</td>
<td>compact disc</td>
</tr>
<tr>
<td>CMOS</td>
<td>complementary metal-oxide semiconductor</td>
</tr>
<tr>
<td>Cu</td>
<td>copper</td>
</tr>
<tr>
<td>CW</td>
<td>continuous wave</td>
</tr>
<tr>
<td>D</td>
<td>drain</td>
</tr>
<tr>
<td>DC</td>
<td>direct current</td>
</tr>
<tr>
<td>DVD</td>
<td>digital versatile disc</td>
</tr>
<tr>
<td>EAS</td>
<td>electronic article surveillance</td>
</tr>
<tr>
<td>EEPROM</td>
<td>electrically erasable programmable read only memory</td>
</tr>
<tr>
<td>EIRP</td>
<td>equivalent isotropic power</td>
</tr>
<tr>
<td>EMC</td>
<td>electromagnetic compatibility</td>
</tr>
<tr>
<td>EMCO</td>
<td>EMCO Elektronik GmbH</td>
</tr>
<tr>
<td>EPC</td>
<td>electronic product code</td>
</tr>
<tr>
<td>ESD</td>
<td>electrostatic discharge</td>
</tr>
<tr>
<td>ETSI</td>
<td>European Telecommunications Standards Institute</td>
</tr>
<tr>
<td>FCC</td>
<td>Federal Communications Commission</td>
</tr>
<tr>
<td>FDTD</td>
<td>finite difference time domain</td>
</tr>
<tr>
<td>FM</td>
<td>frequency modulated</td>
</tr>
<tr>
<td>FR4</td>
<td>flame retardant 4 circuit board</td>
</tr>
<tr>
<td>G</td>
<td>gate</td>
</tr>
<tr>
<td>HF</td>
<td>high frequency</td>
</tr>
<tr>
<td>HFSS</td>
<td>high frequency structure simulator</td>
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<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>HP</td>
<td>Hewlett Packard</td>
</tr>
<tr>
<td>ID</td>
<td>inside diameter</td>
</tr>
<tr>
<td>II</td>
<td>impact ionisation</td>
</tr>
<tr>
<td>ISD</td>
<td>Integrated Silicon Design</td>
</tr>
<tr>
<td>ISO</td>
<td>International Standards Organisation</td>
</tr>
<tr>
<td>L</td>
<td>inductor</td>
</tr>
<tr>
<td>LDD</td>
<td>lightly doped drain</td>
</tr>
<tr>
<td>MoM</td>
<td>method of moments</td>
</tr>
<tr>
<td>MOS</td>
<td>metal-oxide semiconductor</td>
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<tr>
<td>MOSFET</td>
<td>metal oxide field effect transistor</td>
</tr>
<tr>
<td>NMOS</td>
<td>N-type metal oxide semiconductor</td>
</tr>
<tr>
<td>NAND</td>
<td>not AND</td>
</tr>
<tr>
<td>NOR</td>
<td>not OR</td>
</tr>
<tr>
<td>NPN</td>
<td>N-type P-type N-type transistor</td>
</tr>
<tr>
<td>OD</td>
<td>outside diameter</td>
</tr>
<tr>
<td>OTA</td>
<td>operational transconductance amplifier</td>
</tr>
<tr>
<td>PCB</td>
<td>printed circuit board</td>
</tr>
<tr>
<td>PET</td>
<td>polyethylene terephthalate</td>
</tr>
<tr>
<td>PJM</td>
<td>phase jitter modulation</td>
</tr>
<tr>
<td>PM</td>
<td>phase modulation</td>
</tr>
<tr>
<td>PML</td>
<td>perfectly matched layer</td>
</tr>
<tr>
<td>PN</td>
<td>P-type N-type junction</td>
</tr>
<tr>
<td>PNP</td>
<td>P-type N-type P-type transistor</td>
</tr>
<tr>
<td>POR</td>
<td>power-on reset</td>
</tr>
<tr>
<td>ppm</td>
<td>parts per million</td>
</tr>
<tr>
<td>PTFE</td>
<td>polytetrafluoroethylene</td>
</tr>
<tr>
<td>PUR</td>
<td>polyurethane</td>
</tr>
<tr>
<td>PVC</td>
<td>polyvinyl chloride</td>
</tr>
<tr>
<td>Q</td>
<td>quality factor</td>
</tr>
<tr>
<td>r</td>
<td>series resistor</td>
</tr>
<tr>
<td>R</td>
<td>parallel resistor</td>
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<tr>
<td>RF</td>
<td>radio frequency</td>
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<td>RFID</td>
<td>radio frequency identification</td>
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<tr>
<td>RRO</td>
<td>reply-rate oscillator</td>
</tr>
<tr>
<td>RTF</td>
<td>reader-talks-first</td>
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<tr>
<td>S</td>
<td>source</td>
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<tr>
<td>SD</td>
<td>standard deviation</td>
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<td>SCR</td>
<td>silicon controlled rectifier</td>
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<tr>
<td>SEBS</td>
<td>styrene-ethylene/butylene-styrene</td>
</tr>
<tr>
<td>SKU</td>
<td>stock keeping unit</td>
</tr>
<tr>
<td>SMA</td>
<td>subminiature version A</td>
</tr>
<tr>
<td>SPICE</td>
<td>simulation program with integrated circuit emphasis</td>
</tr>
<tr>
<td>T</td>
<td>period</td>
</tr>
<tr>
<td>TE</td>
<td>transverse electric</td>
</tr>
<tr>
<td>TPE</td>
<td>thermoplastic elastomer</td>
</tr>
<tr>
<td>TPR</td>
<td>thermoplastic rubber</td>
</tr>
<tr>
<td>TPU</td>
<td>thermoplastic polyurethane</td>
</tr>
<tr>
<td>UHF</td>
<td>ultra high frequency</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>positive supply node</td>
</tr>
<tr>
<td>V&lt;sub&gt;SS&lt;/sub&gt;</td>
<td>negative supply node</td>
</tr>
<tr>
<td>VSWR</td>
<td>voltage standing wave ratio</td>
</tr>
<tr>
<td>XOR</td>
<td>exclusive OR</td>
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<td>7.1</td>
<td>Return loss of absorbing material</td>
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<td>Antenna impedance at 915 MHz in free space</td>
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<td>Antenna impedance at 915 MHz 3.5 mm above metal</td>
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<td>Deep brass well, 25.5 mm depth</td>
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Chapter 1

Introduction

This chapter provides a description of the background to the field of research, and an outline of the material covered in the thesis. A summary of the contributions to knowledge within the thesis is also presented.
1.1 Background

The consideration of the optimisation of and interaction between antennas, waves, and circuits is an emerging philosophy in the design of electronic labelling systems. This view is in line with methods of economical design which are the focus of designers in many areas of manufacturing. In today’s market there is the ever-increasing demand of more for less, therefore the author has considered the economics of manufacturability of the various electronic label or tag components presented. The work calls upon a diverse knowledge of electrical and electronic engineering principles due to the natural requirements of electronic labelling systems.

A review of the electronic labelling industry or radio frequency identification (RFID) as it is now commonly known, has lead the author to identify several areas in need of attention. The shortcomings of previously designed electronic label system components show that isolated component design results in non-optimum system performance. The specifications for the individual components will be shown to be interdependent. One of the design tasks is to minimise the interactions where possible.

A significant challenge in electronic labelling is to meet the need of an industry requirement. An operating specification generally dictates the geometries of both the system components and their relative placement. Often these geometries cannot be physically realised due to the fundamental constraints of electronic labelling systems. In such a case a compromise of some sort must be made, however, having individually efficient components can lessen the effect of the compromise.

The circuit blocks that are developed can be used in both passive and active tags and each such tag has its place in the real world where field generation limits are imposed for reasons of both human exposure and interference with other radio operators, but the focus is largely on passive tags.

1.2 Outline of the thesis

The first six chapters, on antennas, covers both UHF and HF antennas.

Planar tags are those which have their antennas made from a single layer of conductor on a supporting substrate. The UHF antennas developed are similar to thin-wire type antennas yet have a broad operating band.
A two-part antenna was developed out of the need for a simple non-precise post-process method to apply an RFID chip to an antenna that had been printed or otherwise formed on packaging material. The process does not require tight tolerances or expensive conductive glues of other industry approaches.

Both the planar and two-part tags developed allowed for the tagging of file folders for office document traceability where tags are in close proximity to one another.

A combined UHF and HF antenna was developed to provide an upgrade path for existing users of theft detection to RFID in order to exploit the expanded business capabilities of RFID without compromising the reliability of the HF electronic article surveillance (EAS) systems.

A circular tag antenna to be affixed to a DVD or CD after the disc manufacturing process was developed and accepted as an Australian Innovation Patent. This work has usefully extended the repertoire of appropriate RFID antennas. Additionally a tag loop antenna was developed which has the properties of large physical size but with an effective inductance lower than the loop’s intrinsic inductance. This has led to an antenna which has increased range while maintaining low susceptibility to the detuning factors of its environment.

In Chapter 7, the first of two chapters on waves, the use of a high-frequency magnetic material to increase the UHF field near a metal surface to achieve improved performance of an electric-field-sensitive tag antenna is described.

In Chapter 8, the HF magnetic field inside a metallic hole is investigated, and a tag antenna developed to increase the amount of magnetic field entering the hole and subsequently linking the turns of a tag solenoid antenna. Noise measurements relating to this work are included.

The last five chapters, on circuits, focus primarily on low-complexity circuits used as individual but interrelated building blocks for a passive HF RFID chip.

The circuits include firstly a low-power current reference with immunity to parasitic capacitance, which in some designs can cause oscillation, and which is stable with respect to temperature variations. The circuit is self-starting to ensure operation within the short time a tag can be expected to respond.

Secondly, an unstable oscillator from stable on-chip voltages and currents was developed for the use of a random-number generator. This chapter includes a low-power carrier divider using branch-based logic which was developed for stable local clock generation.

Thirdly, various rectifiers suitable for post-rectifier regulation are examined.
Chapter 1

Fourthly, shunt regulators on the DC side of a chip rectifier were developed as an alternative to or to augment regulation on the RF side.

Lastly, a low-power on-wafer detector which was accepted as an Australian Innovation Patent was developed to allow logic circuits to reconfigure themselves in a manner which depends on whether the chip is on a wafer or is a die from a sawn wafer.

1.3 Original contributions of the author

The following paragraphs summarise the author’s contributions to knowledge.

The development of antennas which are confined to the periphery of a label to allow printing of the label with inventory or retail information without interference from the antenna or chip. The tags are also broadband and perform well in applications where close tag-to-tag spacings exist. A simulation environment was developed to obtain trustworthy results of antenna impedances in a short simulation time.

The development of a two-part antenna system which consists of a first small loop tag which couples to a larger antenna. This is a benefit for RFID manufacturers as it allows them to qualify and keep inventories of a single tag which can be applied to many applications. Product manufacturers may apply the small loop to their products to couple to a larger antenna formed in the product or the product’s packaging using existing process steps. The larger antenna design uses narrow tracks in order to be formed economically from conductive inks or metal-vapour deposition processes. The two-part tags are also broadband and perform well in applications where close tag-to-tag spacings exist. Adjustment of the small loop’s position relative to the larger antenna allows minimisation of mutual tag coupling for book and office applications where very close tag separations exist.

The development of a combined UHF RFID and HF EAS tag which makes maximum use of the available area of a tag without compromising the performance of either UHF or HF feature. The tag further allows the addition of a UHF RFID feature to an HF EAS tag which uses EAS detection infrastructure which may be already in place in a retail application.

Designing a tag for a DVD or CD which performs well in the display arrangements of a retail application where tags are in close proximity to others. The tag design allows it to be applied directly to the disc (so that it cannot be peeled off
An integrated matching network for a UHF loop tag was developed in order to increase the electrical size of a loop for a given physical size. The loop antenna which generates less near electric field is more tolerant to environmental detuning and was suitable for livestock ear tagging.

A simple small tag design was developed for the tagging of metal objects; it used a piece of thin electromagnetic absorber material between the tag and metal to reduce the reflective effects which occur near a metal surface and which normally reduce the available electric field to unusable levels.

An HF ferrite coil was developed for operation inside a hole in a metal object. Simulation results were verified by empirical measurements to gain confidence in the simulated results in order for more-manufacturable coil designs to be developed.

A low-value current reference was developed to be both stable and self-starting for passive RFID chips.

A size-efficient low-power random-number generator was developed for RFID chips which comply with time-slotted anti-collision protocols. The circuit showed a substantially uniform distribution in the random numbers generated.

Rectifiers for passive HF chips were developed in association with DC side regulators which allowed HF tags to survive high magnetic fields without breakdown of diffusions or oxides in CMOS processes. The combination allowed shallow AM modulation to be detected while maintaining fast clamping of internal voltages in cases where a tag moves quickly into a high magnetic field or when a tag is in a position where a high magnetic field is rapidly activated.

Development of a zero-power circuit which detects whether a chip is on a wafer or on a sawn die. The zero-power feature is a contrast to other simple resistive pull-up or pull-down methods. The design was examined and granted an Australian Innovation Patent.
The most common antenna used in RFID is a short dipole constructed from a single conductive layer on a supporting substrate. The conductors of the antenna element thus lie substantially in a single plane. This chapter considers the design and simulation of such antennas and describes the development of antennas with the important properties of broad bandwidth and the ability to be stacked with minimal interaction.
2.1 Introduction

This basic planar element, along with the RFID chip, is often called an “inlay”, since it is able to be inlaid between other decorative or printable layers and a further adhesive layer for attachment to an item.

2.2 Read range

Read range may be represented by the actual distance from the reader antenna for a particular reader and antenna set-up, or by the measured minimum power required to read a tag as if received by an isotropic antenna at the tag location at a fixed distance (EPC Global 2008b) of 0.8 to 1 m. This latter representation is the equivalent isotropic radiated power (EIRP) of the reader and reader antenna system minus the propagation loss from the reader antenna to the tag location.

The measurement is performed in an anechoic chamber with a reader containing an in-phase and quadrature demodulator in the receiver, power is ramped up from a low level until the tag response is detected, the reader power level is recorded and adjustments for the reader antenna factor and propagation loss are applied to result in a minimum power level at the tag position for a tag reply. This is a good way to compare tags since the hardware is constant and there are no (or at least consistent) reflections, whereas outdoor measurements even though performed with constant hardware over a constant range tend to vary with weather conditions, which through varying moisture content can affect ground reflections.

2.3 RFID antenna impedance

The first details required to design an antenna are to identify the operating frequency and antenna impedance required for attachment to the RFID chip. The loads presented by UHF RFID chips are capacitive, due to the capacitance of the diodes used for rectifying the RF to a DC for powering the chip electronics. In regards to the antenna impedance, the desired impedance is that which results in the best tag read range, which does not necessarily occur at the complex conjugate of the RFID chip’s input impedance. There are two main reasons for the difference. Primarily it is due to the RFID chip changing its input impedance when it modulates, essentially adding some lossy capacitance to shift the chip impedance to a lower reactance. Secondary to this the RFID chip has to be assembled to the
Table 2.1. Impinj Monza2 chip impedance, single-ended (1-port).

<table>
<thead>
<tr>
<th>frequency</th>
<th>antenna impedance</th>
</tr>
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<tbody>
<tr>
<td>866 MHz</td>
<td>58 + j166 Ω</td>
</tr>
<tr>
<td>915 MHz</td>
<td>52 + j158 Ω</td>
</tr>
<tr>
<td>956 MHz</td>
<td>48 + j153 Ω</td>
</tr>
</tbody>
</table>

Table 2.2. NXP Ucode G2XM chip data.

<table>
<thead>
<tr>
<th>frequency</th>
<th>chip impedance</th>
<th>assembly parasitic</th>
</tr>
</thead>
<tbody>
<tr>
<td>915 MHz</td>
<td>22 - j195 Ω</td>
<td>20.5 Ω in series with 0.309 pF</td>
</tr>
</tbody>
</table>

antenna which for flip-chip assembly results in a lossy shunt capacitance placed across the RFID chip terminals.

Parasitic capacitance aside, matching the antenna to the RFID chip results in the tag activating at long range but its excitation collapsing during modulation, hence the tag fails to be read. The antenna impedance is a compromise, and in all the RFID chips the author has tested the best antenna impedance had an inductive reactive part of lesser magnitude than the chip’s conjugate match.

Each manufacturer has their own way of writing data sheets and presenting chip impedance data. Impinj, who manufacture the Monza2 and Monza4 UHF Gen 2 compliant chips (EPC Global 2008a), state target antenna impedances for best range and provide a Smith chart with impedance contours where the reader excitation power must be increased by a specific number of dB in order to maintain range. An example of antenna impedance data for the Monza2 chip is shown in Table 2.1. For the same chip, Figure 2.1 shows a Smith chart indicating points of ideal antenna impedance for shunt, single-ended (one-port) and differential connection of the chip’s two input ports. A contour of the antenna impedances which result in 1 dB more power than the minimum to energise the chip into operation for the single-ended (SE) connection is also shown in Figure 2.1.

NXP, formerly Philips, who manufacture the Gen 2 compliant Ucode G2XM chip, state chip impedances and suggest assembly parasitics, such as those stated in Table 2.2, and provide an antenna design guide with performance results so the reader may deduce what antenna impedances result in what read range. Simulation results for the NXP reference antenna illustrated in Figure 2.2 are shown in Figure 2.3.
Figure 2.1. Impinj Monza2 chip Smith chart with contour of impedances which require 1 dB more input power when in the one-port or single-ended (SE) configuration.

Figure 2.2. NXP’s reference antenna for the Ucode G2XM chip.

Figure 2.4 shows the measured minimum power, as discussed in Section 2.2, for 8 tags formed by mounting NXP G2XM chips on their suggested reference antennas and tested as outlined in Section 2.2.

The design of a tag antenna to achieve the desired tag impedance normally proceeds by simulation. The question of calibrating the simulator therefore arises.
Figure 2.3. NXP's reference antenna for the Ucode G2XM chip: Simulation (left axis reactance $\Omega$ in blue; right axis resistance $\Omega$ in red).

Figure 2.4. NXP's reference antenna with the Ucode G2XM chip: Measured minimum power as if received from an isotropic antenna at the tag position for 8 reference tags.
2.4 Calibrating the simulator

The Ansoft HFSS simulator is widely used for antenna simulations. The way in which it was used for this work was to look at the antenna from a 50 Ω source, as if the antenna was connected to a network analyser. An antenna would be designed to a target impedance, and then physically realised with conductors on a supporting substrate with an aspect of the antenna made longer than required, typically the overall length of a straight dipole around one half wavelength long, or the length of a shorter dipole with folded back capacitive antenna ends. The trimmable antenna section is then incrementally cut back with a knife and read range (or minimum operating power at a fixed range), determined experimentally using the method described in Section 2.2, is recorded against the physical measured length of the trimmable feature. When the read range passes through a maximum, the physical length for the maximum is entered into the simulated design. An impedance point for the antenna and a particular chip is then known to give good read range.

Further testing allows fine tuning of the process, and the antenna design can be modified to yield an antenna with an input impedance suitable for the particular type of RFID chip. In this way of testing it really doesn’t matter if there are small discrepancies between the impedance reported by simulation and the impedance that may be measured directly with a network analyser, but analyser measurements almost always involve some kind of test jig and careful connection to maintain parasitic capacitances.

To initially get a level of confidence in the simulator for more arbitrary shaped antennas, the simulation environment was set up to include a volume surrounding the antenna, this volume being small enough to keep the number of spatial simulation points or line meshes within the volume small, but large enough for realistic near fields to have reduced to a low level before encountering the simulation volume boundary. This technique provides accurate results in a reasonable simulation time.

2.4.1 The Balanis dipole analysis

The Balanis (Balanis 1982) thin-wire dipole analysis based on the method of moments (MoM) was chosen as a reference for the simulation space since it is well-characterised and was about the longest structure intended to be investigated. Convergence of Balanis’ delta-gap and magnetic-frill methods occurred when a
half-wave dipole was divided into 61 or more segments. For a XFDTD\(^1\) method to agree with Balanis’ delta-gap method, 29 or more segments were required.

Using a simulation frequency of 915 MHz, a 0.47\(\lambda\) long, 0.005\(\lambda\) radius solid copper dipole was laid out. Instead of dividing the antenna into segments as in Balanis’ MoM analysis, HFSS uses meshes to represent solids and surfaces. These meshes can be restricted in their number or their size.

Since the mesh length resembles the segments used in Balanis’ moment method, a half-wave dipole at the upper frequency of interest, 956 MHz, was divided into 61 segments to give a rounded down maximum mesh length of 2.4 mm. Any conductive antenna surface would thus use this maximum mesh length of 2.4 mm for the meshes used to represent the surface. In this way, currents were approximated to be uniform along a mesh line which could not be any longer than the segments used for a convergent solution in Balanis’ analysis.

The simulator has provision to surround a structure with a perfectly matched layer (PML) which offers a reflection-free interface between the air (or space) and the PML layer as far as propagating modes are concerned. The use of these layers in a walled cage around the design allows the design space to be shrunk from what it would need to be for a radiation-surface type simulation which requires enough space for the propagating fields to develop, around 1\(\lambda\) resulting in a very large simulation space. Although such simulations were performed in early work, the simulation times were very long. To overcome this limitation the following method was implemented.

Using the concept of the radian sphere (Wheeler 1959) where 
\[ r_{\text{radiansphere}} = \frac{\lambda}{2\pi}, \]

a cube was created with 2\(r_{\text{radiansphere}}\) distance between the cube and the antenna. This allows the majority of the near fields to develop within the cube before our PML layer is encountered. A thickness of the PML layers used was 2\(r_{\text{radiansphere}}/3\) to keep the overall simulation space as confined as possible with good accuracy, and the lowest frequency parameter for the PML calculation was chosen as 800 MHz, since 866 MHz is the lowest RFID band.

The space surrounding the antenna was limited to between 1000 to 2000 points (lower for smaller structures). The simulator was set up with a convergence criterion of 2 % variation in impedance values between iterations before convergence could be declared, with a minimum of 3 iterations. Between 1 to 10 % of the worst converging meshes would be recalculated before the next simulation iteration.

\(^1\)A three-dimensional full wave electromagnetic solver based on the finite difference time domain method (FDTD).
Table 2.3. Impedance results for a 61 segment dipole of length $0.47\lambda$ and radius $0.005\lambda$ in free space.

<table>
<thead>
<tr>
<th>method</th>
<th>MoM Δ-gap</th>
<th>MoM mag.-frill</th>
<th>XFDTD</th>
<th>HFSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>impedance</td>
<td>78.6 + j6.1 Ω</td>
<td>76.2 + j8.5 Ω</td>
<td>77.7 + j5.3 Ω</td>
<td>77.5 + j8.4 Ω</td>
</tr>
</tbody>
</table>

These simulation parameters provided antenna input impedance values in good agreement with Balanis’ results, and a fast simulation time. This meant other form factor antennas could be designed by adjusting various physical dimensions to see how those changes impacted on the input impedance.

The impedance results for the $0.47\lambda$ dipole in 61 segments from Balanis’ work by two MoM methods, some internet (Remcom 2004) results, and my HFSS\(^2\) results are shown in Table 2.3.

The accuracy achieved for the impedance results allowed some degree of confidence in comparing design ideas. Antenna efficiency was thought not be highly accurate for small electrical length antennas, but relative changes in simulation efficiency were reflected in empirical comparisons of tested antennas when small changes to an antenna design were made to maintain impedance and maximise efficiency. The HFSS simulator also provided as one of its outputs an estimate of 99.729% antenna efficiency for the $0.47\lambda$ long, $0.005\lambda$ radius solid copper dipole, and as the following analysis shows, the developed simulation environment gave confidence in the ability to tweak certain parameters of an antenna design to ultimately achieve good read range.

### 2.4.2 Loss calculation of a half-wave dipole

For an antenna of length $l$ and radius $r$ made from material of conductivity $\sigma$ and skin depth $\delta$ with end points of $-l/2$ and $l/2$ along the $z$ axis the current at position $z$ is:

$$I(z) = I_p \sin[\beta(l/2 - |z|)]$$

The power dissipated in a differential length $dz$ is given by:

$$dP = \frac{I_p^2}{\sigma A} dz$$

where $A = 2\pi r \delta$

$$dP = \frac{I_p^2}{2\sigma A} \sin^2[\beta(l/2 - |z|)] \, dz$$

\(^2\)Mesh operation: antenna maximum length 2.4 mm; space maximum elements 2000; lambda refinement 0.05 free-space lambda.
So the total power dissipated is:

\[ P = \int_{-l/2}^{l/2} \frac{I_p^2}{2 \sigma A} \sin^2[\beta(l/2 - |z|)] \, dz \]

Substituting \( u = \beta (l/2 - z) \) and \( du = -\beta \, dz \)

\[ P = \int_{\beta l/2}^{0} - \frac{I_p^2}{\beta \sigma A} \sin^2 u \, du \]

Using \( \int \sin^2 u \, du = \frac{1}{2} u - \frac{1}{4} \sin(2u) \)

\[ P = \left[ - \frac{I_p^2}{\beta \sigma A} \left( \frac{1}{2} u - \frac{1}{4} \sin(2u) \right) \right]_{\beta l/2}^{0} \]

\[ P = \frac{I_p^2}{\beta \sigma A} \left( \frac{\beta l}{4} - \frac{\sin(\beta l)}{4} \right) \quad (2.1) \]

For operation at \( f = 915 \) MHz we used the same inputs as in Balanis' analysis:
\( \lambda = 328 \) mm, \( l = 0.47 \lambda = 154 \) mm, \( r = 0.005 \lambda = 1.64 \) mm, \( \sigma_{Cu} = 58 \times 10^6 \) S/m, \( \delta_{Cu} = 66.1 / \sqrt{f} \) mm = 2.19 \( \mu \)m, \( \beta = 19.16 \) rad/m, \( A = 2\pi r\delta = 22.57 \times 10^{-9} \) m\(^2\).

The feed-point current \( I_0 \) is:

\[ I_0 = I_p \sin[\beta(l/2 - |z|)] \quad \text{with } z = 0 \]

So:

\[ I_0 = I_p \sin \left( \frac{\beta l}{2} \right) \quad (2.2) \]

Using \( P = \frac{1}{2} I_0^2 R_I \) where \( R_I \) is the input resistance, rearranging for \( R_I \):

\[ R_I = \frac{2P}{I_0^2} \quad (2.3) \]

Substituting 2.2 and 2.3 into 2.1:

\[ R_I = \frac{2}{\beta \sigma A \sin^2 \left( \frac{\beta l}{2} \right)} \left( \frac{\beta l}{4} - \frac{\sin(\beta l)}{4} \right) \]

Substituting using the dimensions and material properties given above gives:

\[ R_I = 61.35 \times 10^{-3} \, \Omega \]
As a check the DC resistance and the AC resistance (uniform current distribution) were calculated. The calculated $R_l$ was greater than the DC resistance and less than the uniform current AC resistance as expected.

\[
R_{\text{DC}} = \frac{l}{\sigma \pi r^2} = 314.24 \times 10^{-6} \, \Omega \\
R_{\text{AC}} = \frac{l}{\sigma 2\pi r \delta} = 117.66 \times 10^{-3} \, \Omega
\]

Using the analytical result (Sadiku 1989a) for $R_{\text{rad}}$ of 73 $\Omega$ and the following relation the antenna efficiency was calculated:

\[
\eta = \frac{R_{\text{rad}}}{R_{\text{rad}} + R_l} = \frac{73}{73 + 0.06135} = 99.916 \%
\]

This analytical result of 99.916 % compared to the 99.729 % found in simulation meant the simulation environment did not yield anything too unrealistic. From one of the outputs of the HFSS simulator, the simulated directivity for the antenna was 1.6427 which again is close to the accepted 1.64 for a half-wave dipole. The developed simulation space was considered to give representative results of a physical antenna.

### 2.5 Shortening the antenna

With a half-wave dipole being around 162 mm long, and applications tending to favour shorter antennas (less than 100 mm), the dipole cannot be simply fed at a gap at the symmetry point, as the short antenna’s capacitive reactance must be matched to the RFID chip reactance which is also capacitive. This section is concerned with providing the resonating inductance and coupling it to a shortened antenna.

The equivalent diameter (Johnson 1993a) $d$ of flat thin conductors of width $w$ can be found using the relation $d = w/2$. The basic antenna conductor is a track of
aluminium, copper, or silver ink with a width around 1 to 4 mm giving a range for the equivalent diameter of 0.5 to 2 mm. Tracks are favoured due to flexibility in being able to reuse designs with various antenna manufacturing methods such as conductive ink and metal-vapour deposition. Traditional etching is still possible for tracks, but large areas of conductor are avoided to maintain the ability to use additive methods for the formation of antenna conductors.

Using a starting antenna length of 100 mm (a half-antenna length of around 55 degrees) the ratios of length to diameter (Johnson 1993b) from 50 to 200 yield antenna impedances of around 5 \( \Omega \) in the real part and \(-j140\) to \(-j200\) \( \Omega \) in the imaginary part. Placing the chip at a gap at the dipole’s symmetry point and adding a shunt inductor allows us to tune the feed point to a reactance around \( j200 \) \( \Omega \), and to a resistance of 8 to 9 \( \Omega \). If we change the shape of the shunt inductor we can alter its connection points to the dipole changing the antenna feed-point resistance while maintaining the inductance needed to give the required feed-point reactance.

Experimentation with moving the connection points resulted in tunable antennas but not enough flexibility in obtaining the desired resistance value. Resistance values around 20 to 30 \( \Omega \), usually higher than the RFID chip resistance, are desired for a tag offering good operating bandwidth and immunity to the surface material the tag may be mounted on or near during its operation.

So for flexibility in matching, the basic antenna as shown in Figure 2.5 was used. The antenna is an electrically short dipole with no gap, coupled to a loop which connects to a capacitive chip; the loop provides a suitable inductance and the spacing between the loop and the dipole allows adjustment of the antenna resistance seen by the chip. More coupling pushes the resistance value upwards, and some designs require no spacing between the loop and the dipole. This “no spacing” is achieved by merging the loop with the dipole or, as seen later in Chapter 3, by overlapping the loop with the dipole of a two-part antenna either on an insulating substrate side or a completely separate substrate. In this latter case the antenna can have a resistance greater than that which is achievable by merging the loop with the dipole section. This is important for a small tag when the dipole is small (around 50 mm) and has a low unmatched resistance.
2.6 Dipole with a loop

The dipole-with-a-loop antenna type turns out to be quite common with RFID manufacturers, and was chosen for a first investigation. The loop forms a shunt DC path for the chip which was required for early RFID chips using single diode half-wave rectifiers, but nowadays RFID chips are monolithic and commonly use full-wave or voltage-doubler rectifiers, or in any case do not require a DC path.

A first benefit noticed from the design illustrated in Figure 2.5, which had impedance characteristics similar to those illustrated in Figure 2.3, is the inflection in the reactance curve when the impedance is plotted against frequency. Looking at Table 2.1 it is noticed that the reactance of the best antenna impedance drops with frequency. A loop, or a half-wave dipole, has a reactance that increases with frequency as is shown in the left half of Figure 2.3. In order for a broadband match the antenna reactance should decrease with frequency. Having a broadband antenna seemed a good design target since the RFID frequencies are not uniform across the world. So it appeared that arranging for the inflection to be at the mid-band frequency (for example 915 MHz for the 902 to 928 MHz FCC band) should yield good read range across the whole RFID band.

A second design criterion is the type of surface that the tag will be affixed to when an item is tagged. A design for a library or retail book provides a challenge since
books vary in thickness and some have decorative plastic layers on the cover. The form factor chosen in our work is to fit within an industry standard label used for the traditional printed barcode. Also, the books to be equipped with RFID still require legacy barcodes and pricing information to be printed on the label, so an open C-shaped form such as shown in Figure 2.6 of overall dimensions of 71 mm × 32 mm is chosen. This form turns out to be a good choice for reasons of the antenna quality factor.

Other tags used in RFID are substantially two-dimensional or planar versions of three-dimensional antennas. An example is shown in Figure 2.7.

The small three-dimensional antenna which makes the best use of the available volume (Johnson 1993b) is shown in Figure 2.8. The antenna has cylindrical caps supported by a coil which makes maximum use of the antenna’s physical volume without increasing the occupied cylindrical space. The author has found that this type of antenna when projected on to a plane, to form a substantially two-dimensional or planar antenna as shown in Figure 2.7, does not make the best use of the available area.
Figure 2.7. Example of a 3-dimensional antenna represented in 2 dimensions.

Figure 2.8. A small 3-dimensional antenna.
For the planar antenna case the results are:

- a capacitive top does help bandwidth;
- a skirt of length one quarter of the dipole length on the capacitive top does help bandwidth but is only required on one side; and
- a loading coil doesn’t help but instead hurts bandwidth.

The dipole antenna can be represented as a series rLC circuit. We can get a relation for the quality factor as follows.

\[ \omega = \frac{1}{\sqrt{LC}} \]  
\[ Q = \frac{\omega L}{r} = \frac{L}{r\sqrt{LC}} = \frac{\sqrt{\frac{L}{C}}}{r} \]  

So from Equation 2.5 we can lower the quality factor and hence broaden the bandwidth by a number of techniques. One is increasing the radiation resistance by using a longer dipole, but this option is unavailable in a tag of constrained size. Another is transforming a low radiation resistance upwards. A third is by reducing the ratio of \( L/C \) while maintaining the product \( LC \) to keep the resonant frequency constant. This result is achieved with a fat wire dipole which has an equivalent circuit with less inductance and a larger capacitance than a thinner wire dipole, and thus achieves a broader bandwidth.

Figure 2.6 shows a C-shaped antenna designed for operation on a book. The loop and chip connection are indented towards the dipole due to restrictions placed on the chip location by the printer mechanism which step feeds, prints human readable information, and dispenses the tags which are within sticky-backed paper labels, and will conduct operations very close to the loop.

Again, Equation 2.5 suggests that the C-shaped antenna of Figure 2.6 should be a good broadband performer compared to other RFID antennas containing serpentine or meander-line tracks which increase the electrical length and provide inductive reactance, since the inductance of the main dipole segment is small (a straight wide track) and larger capacitive ends have been placed at the ends of the main segment to “top load” the dipole increasing the effective electrical length (Terman 1943).
2.6.1 Modelling a book

A median size book for tag testing was the Code of Federal Regulations 47 Parts 0 to 19, 230 mm × 150 mm × 30 mm, dense white paper (as compared to pulp) with a thicker paper cover, chosen since it is commonly found in RFID laboratories. A basic tag was designed for operation in air, but made with the capacitive skirts at both ends of the C-shape, as shown in Figure 2.9, a little longer than required for the simulated value of a first guess of the required reactance (a guess is required because capacitances associated with chip attachment are not yet accurately taken into account and furthermore chip impedances vary) and a resistance around the equivalent series resistance of the chip.

This tag's skirt was trimmed for best read range in a laboratory measurement, the trimmed version was then simulated to get a refined design point of the reactance. Tweaking of the resistive part will help from here in terms of improving the bandwidth but has little effect on the reactance for best range. The tag was then placed on to the book and the length of the capacitive skirt was further trimmed for the best read range in a laboratory measurement. The trimmed version of the tag was then simulated with a slab of paper representing the book placed under the tag with the book paper dielectric constant as a parameter, and this dielectric constant adjusted until the reactance was the same as that for the tag in air.
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Figure 2.10. Simulated impedance for a 71 mm × 32 mm tag antenna designed for use on a 30 mm thick book with an NXP Ucode G2XM chip.

The 30 mm slab of “book paper” was modelled by $\varepsilon_r = 2.35$ and $\tan\delta = 0.005$ (electric). Using this single slab keeps the simulation of a book simple, as using many thinner slabs with air gaps to model the book would require a lot of mesh lines, as each thinner slab requires its own meshes. The impedance results are shown in Figure 2.10.

Normal paper was modelled using $\varepsilon_r = 3.0$ and $\tan\delta = 0.005$ (electric), for retail labels (that usually also carry a barcode) and manilla folders that contain documents. A 30 mm thick book could also be modelled in simulation by using the physical parameters of normal paper but representing the book’s pages to an equivalent solid slab with a thickness of 6.5 mm.

The designed tag was then tested on a range of materials each 10 mm thick (see Table 2.4). Figure 2.11 shows the minimum input power for tag operation obtained by laboratory measurements for air and three materials. The material slabs measured 240 mm × 125 mm × 10 mm. A 10 mm thick slab of PTFE with $\varepsilon_r = 2.06$, and $\tan\delta = 0.001$ (electric), gave similar results to those of a simulated slab of 6.5 mm thick paper with $\varepsilon_r = 3.0$. The measured results show a good broadband performance for PTFE, and also good performance with higher dielectric constants. This means the tag can cope with books of varying thicknesses with plastic or plastic-coated book covers.
Table 2.4. Dielectric constants for various materials.

<table>
<thead>
<tr>
<th>Material</th>
<th>$\epsilon_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Air</td>
<td>1</td>
</tr>
<tr>
<td>Polytetrafluoroethylene (PTFE)</td>
<td>2.12 to 2.2</td>
</tr>
<tr>
<td>Polyurethane (PUR)</td>
<td>4.05 to 4.12</td>
</tr>
<tr>
<td>Carbon-amide reinforced plastic (CARP)</td>
<td>5.78 to 5.87</td>
</tr>
</tbody>
</table>

Figure 2.11. Measured minimum power as if received from an isotropic antenna at the tag position for a tag antenna designed for a book tested on various surfaces.

The broadband result for air was a little surprising because the tag had been designed for placement on a book and removal of the dielectric material would move the features shown in Figure 2.10 to higher frequencies but as it turned out the reactive part of the impedance as seen in Figure 2.12 was still quite suitable over the frequency range, only the resistive part was lower and gave the overall lower range. Although the materials add loss, overall the match to the RFID chip is better when the tag is on dielectric material as shown in Figure 2.10.
Figure 2.12. Simulated impedance for a 71 mm × 32 mm book tag antenna designed for use with an NXP Ucode G2XM chip but in air.

### 2.7 Close-coupled tags

Placing a tag in a book inevitably results in tags being in close proximity with others, around 3 mm apart for thin children’s books, as they are stacked on a shelf or packed in a box. Applications such as office files or records require tags to be spaced close together, with separation distances as small as 1 mm. The two-part tag, discussed in Chapter 3, was thought suitable for this application since the folder or paper could function as the supporting substrate of a secondary antenna printed directly on to it using silver ink, and the antenna is RFID enabled by sticking a smaller primary antenna to the supporting substrate in the vicinity of the secondary antenna.

RFID antennas may be modelled in a simple way (Horn et al. 2000) by an inductor. Figure 2.13 shows the two inductors of two antennas along with parasitic capacitances whose connections have been approximated to reside at the ends of the inductors. The analysis uses the weak coupling approximation, i.e. coupling where the influence of a first antenna is considered on a second but the second’s influence back on the first is ignored.

Figure 2.14 shows: a voltage generator in series with the second inductor which represents the influence of the first antenna on the second due to mutual inductance; and a current generator which represents a shunt current path across the
Figure 2.13. Two tag antennas modelled as inductors with parasitic capacitances.

Figure 2.14. The influence of one tag on another.

Second inductor provided by the parasitic capacitances between the two antennas.

\[
V_{im} = j\omega MI_1 \\
I_{iC} = j\omega CV_1 \\
= j\omega Cj\omega LI_1
\]

The current generator is converted into a second series voltage acting on the second inductor.

\[
\frac{V_{iC}}{j\omega L} = I_{iC} \\
V_{iC} = j\omega LI_{iC} \\
= j\omega Lj\omega Cj\omega LI_1
\]
This can be made to cancel with $V_{im}$ when:

$$\omega M - \omega L C \omega L = 0$$

$$C = \frac{M}{(\omega L)^2}$$

So with the right amount of parasitic capacitance between the two antennas, it is possible for the first antenna to have no coupling to the second. In practice, changing the antenna structure to include parasitic capacitance minimises the influence between close-coupled tags.

To design a tag which would operate by itself and amongst others as the case would be for thin books or files, the mutual impedance between antennas is minimised. The ports of each antenna were terminated in 50 $\Omega$, as if connected to a network analyser. For a group of $n$ antennas:

$$V_i = \sum_{j=1}^{n} Z_{ij} I_j \quad i = 1, 2, ..., n$$

By minimising the mutual terms while still maintaining an overall input impedance suitable for good single tag performance, a 71 mm $\times$ 32 mm design was found in which all tags could be read in a packed box of 70 books each 3 mm thick, and a 50 mm $\times$ 30 mm design allowed a stack of 20 files each 1 mm thick to be read also.

When comparing tags of different designs, two tags of each design were simulated at a separation depending on the application, and the ratio of the magnitudes of the imaginary parts of $Z_{21}$ to $Z_{11}$ were compared. This proved useful as it is simpler to simulate only two tags, and empirical results obtained by testing a group of tags showed that the better tag was in fact the one with the lowest ratio of magnitudes of the imaginary parts of $Z_{21}$ to $Z_{11}$.

Figure 2.15 shows the operating bandwidth for a stack of 5 book tags 71 mm $\times$ 32 mm separated in air (foam) by 10 mm. The stack was arranged like a stacked deck of cards with space between the cards, the centre of each tag was spaced on a common line with the tags’ larger dimensions in parallel planes. In simulation, there was an inductive mutual reactance between two tags with separations from 1 to 10 mm.

A smaller 50 mm $\times$ 30 mm tag designed for files and clothing in fact showed simulated capacitive mutual reactance between two tags with separations from 1 to 10 mm. A similar stack of tags showed a larger operating bandwidth with tags in close proximity as seen in Figure 2.16. The mutual reactance became inductive.
with larger spacing, so in a large stack of tags the additions of capacitive and inductive mutual reactances over a small fraction of a wavelength resulted in good tag tuning within the stack, while an isolated tag would still perform since its isolated impedance had not been so compromised for operation in a stack that left it unusable in isolation.

Tags with inductive mutual reactance to the next tag in a stack over larger fractions of a wavelength such as in half-wave dipoles (Johnson 1993a) result in a design which must have a reduced inductive reactance in isolation so that operation within a stack is possible. A factor which tends to reduce the effect of the isolated tag’s compromised tuning is that the larger 71 mm $\times$ 32 mm antenna, because of its greater length, is a more-efficient radiator.

Figure 2.17 shows the mutual reactance between two similar tag antennas, separated in air. What was noted was that the 50 mm $\times$ 30 mm design which was designed for close coupling in applications, such as labelling files, had significant capacitive mutual reactance when in air. This effect can explain the tag’s good
performance in the stack of files, the file paper tends to load the antenna shifting the resonant frequency down, and the mutual capacitance raises the resonant frequency compensating for the paper.

### 2.8 A two-port tag

A baggage tag was required to be read when a patron places luggage on to a conveyor with a plastic encapsulated tag attached via a lanyard, hence the tag will dangle and the orientation to a reader antenna under the conveyor is unknown. The tag was thus required to be omnidirectional. Features of the Impinj Monza2 and Monza4 RFID chips are two independent ports for both powering and load modulating. Therefore two orthogonal antennas may each be connected to one of these input ports to yield an antenna which can be read in any orientation from a circularly polarised reader antenna.

The encapsulation was in the form of a wheel and tyre, a disc of 80 mm in diameter merged with a torus of 80 mm OD and 9 mm section diameter. The function of the torus piece was to prevent the tag from laying flat against the luggage, giving
Figure 2.17. Mutual reactance between pairs of inlay tags.
some spacing between the antenna and the material surfaces of the luggage, and for decorative reasons was over-moulded in thermoplastic polyurethane (TPU), a softer material than the acrylonitrile butadiene styrene (ABS) main section.

The antenna design to be considered was based on the success of the dipole coupled to a loop with the RFID chip, but two orthogonally crossed dipoles would be used. In order to keep the design symmetrical the C-shaped dipole antenna could not be used, so an I-shaped dipole, formed by two T-shaped capacitive top-loaded dipole halves was used.

The overall tag diameter was eventually chosen to be 63 mm. Larger diameter prototypes were tried however it was found that consistent tuning could be achieved by keeping the capacitive loaded antenna ends clear of the outer TPU ring of the tag case.

Small 10 mm × 10 mm capacitors were made from various over-mould materials so that the electric loss factor (see Table 2.5 and Table 2.6) of the materials could be compared.

<table>
<thead>
<tr>
<th>Material</th>
<th>Descriptor</th>
<th>Colour</th>
<th>$Q_{930,MHz}$</th>
<th>$\tan\delta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPU</td>
<td>J unknown degree</td>
<td>black</td>
<td>7.4</td>
<td>0.135</td>
</tr>
<tr>
<td>TPU</td>
<td>ML unknown degree sample1</td>
<td>white</td>
<td>19.0</td>
<td>0.053</td>
</tr>
<tr>
<td>TPU</td>
<td>ML unknown degree sample2</td>
<td>white</td>
<td>15.2</td>
<td>0.066</td>
</tr>
<tr>
<td>TPU</td>
<td>80 % current ML</td>
<td>grey</td>
<td>6.9</td>
<td>0.145</td>
</tr>
<tr>
<td>TPU</td>
<td>80 % another ML</td>
<td>white</td>
<td>7.6</td>
<td>0.132</td>
</tr>
<tr>
<td>TPU</td>
<td>80 % A</td>
<td>white</td>
<td>9.0</td>
<td>0.111</td>
</tr>
<tr>
<td>TPU</td>
<td>80 % from vendor</td>
<td>white</td>
<td>8.0</td>
<td>0.125</td>
</tr>
<tr>
<td>TPU</td>
<td>70 % from vendor</td>
<td>grey</td>
<td>6.5</td>
<td>0.154</td>
</tr>
<tr>
<td>TPE</td>
<td>65 %</td>
<td>white</td>
<td>22.3</td>
<td>0.045</td>
</tr>
<tr>
<td>TPE</td>
<td>90 % coolgrey11c from vendor</td>
<td>grey</td>
<td>9.5</td>
<td>0.105</td>
</tr>
<tr>
<td>ABS</td>
<td>vendor</td>
<td>white</td>
<td>26.0</td>
<td>0.038</td>
</tr>
<tr>
<td>ABS</td>
<td>from SIM card</td>
<td>white</td>
<td>33.5</td>
<td>0.030</td>
</tr>
<tr>
<td>ABS</td>
<td>sample from vendor</td>
<td>grey</td>
<td>15.6</td>
<td>0.064</td>
</tr>
<tr>
<td>SEBS</td>
<td>80 %</td>
<td>clear</td>
<td>16.0</td>
<td>0.063</td>
</tr>
<tr>
<td>TPR</td>
<td>J</td>
<td>white</td>
<td>9.9</td>
<td>0.101</td>
</tr>
<tr>
<td>TPR</td>
<td>J</td>
<td>black</td>
<td>10.9</td>
<td>0.092</td>
</tr>
</tbody>
</table>
Other materials were thermoplastic elastomer (TPE), thermoplastic rubber (TPR), and styrene-ethylene/butylene-styrene (SEBS). The capacitor Q was calculated as the measured reactance divided by the resistance at 930 MHz, and the loss tangent tanδ (electric) calculated as 1/Q.

SEBS material resulted in the best performance, however TPU was finally chosen for its mechanical properties, softer with a less-greasy feeling. The increased dielectric constant of the ABS case (εr = 2.8) and the TPU over-moulding (εr = 6) along with small inconsistencies of the sandwiching of the tag within two ABS halves and then the TPU over-mould, along with small positional tolerances of die cut locators in the tag substrate with pillars in the ABS case meant that keeping the antenna’s sensitive capacitive ends clear of the over-mould was a good choice.

Figure 2.18 shows a prototype tag antenna which was placed between two taped-together disc halves of 1.5 mm thick polyvinyl chloride (PVC) plastic.

![Figure 2.18. 70 mm diameter prototype reference antenna.](image-url)
Figure 2.19. 63 mm diameter final antenna.

Figure 2.19 shows the final tag antenna which was encapsulated in an ABS case. Both antennas were designed for the Impinj Monza4 chip which likes an antenna impedance of $25 + j141 \, \Omega$.

Figure 2.20 shows the antenna and substrate, designed and registered (Hall 2011) by the author.
The centre frequency was 922 MHz since the tag was targeted for the Australian UHF band 918 to 926 MHz.

The design technique for the two-port chip was to leave one port open-circuit in the simulation and tune as if the antenna was for a normal single-port chip.

The empirical trimming performed using a linear reader antenna and finding the best read range while performing the trimming on both antenna axes by cutting the ends of the antenna with a knife. The tag was housed in an encapsulation which had been parted with a knife and held back together using tape. The tag would drop its frequency for maximum range by about 2 MHz when actually encapsulated in the ultrasonically welded case, compared to just being taped together and this was taken into account for final redesign. Once trimmed, new inlays were produced, fully encapsulated, and checked for final tuning.

Crossed conductors in a loop was used to connect the chips two input ports to a loop which would couple to a loop at the centre of a pair of crossed dipoles. The spacing between the loops could be adjusted to achieve the required amount of antenna resistance to match to the chip.

The track width was chosen as 1 mm, wide enough for 9 to 18 µm aluminium on 50 µm polyethylene terephthalate (PET), and allowed the smallest outer loop region to keep the main part of the dipole as long as possible while still providing enough inner loop area for the required antenna reactance.

Treatment of the top-load capacitors followed the developed rules of keeping a 4 mm space between conductors (since it would operate in plastic not air) to minimise parasitics. We kept the overall capacitive skirt region less than one quarter of the overall dipole height and following a radial. We made the length of the ends of the capacitive region (which would be trimmed shorter to empirically find the best tuning) a function of an angle, in this case following a constant diameter back towards the main centre conductor. These things made the best use of the available area (Johnson 1993b), and promote angular symmetry (Johnson 1993c) thereby increasing the operating bandwidth.

Figure 2.21 shows a power measurement at different frequencies of the final encapsulated tag. The tag Ref. was the 70 mm prototype in PVC, and the other tags are samples of the final 63 mm antenna. The antenna plane was parallel to the plane of a patch antenna with 6 dBi gain.
Figure 2.21. Measured minimum tag input power vs frequency of the final encapsulated tag.

2.9 Summary

The concept of a thin-wire dipole folded into a C-shape to form capacitive ends, coupled either directly or electromagnetically to a loop connected to the RFID chip was found to allow a good impedance match between chip and antenna while producing a broad enough bandwidth to allow operation from 850 to 950 MHz using antennas with a maximum dimension of 50 mm. The concept was extended to a dual-port chip which with two orthogonal antenna elements allowed full three-dimensional operation when excited from a circularly polarised reader antenna.
Chapter 3

A Two-Part UHF Antenna

This chapter describes an inexpensive method of tag construction where the completed tag is comprised of a first part containing a small primary antenna and a data-carrying device, and a second part which contains a larger secondary. The two-part tag not only has manufacturing advantages but works well in close-coupled applications where tags are stacked.


### 3.1 Introduction

Manufacturing expenses have a large influence on the number of discrete tag product lines RFID vendors offer, which often results in the use of a common tag form factor being used on various types of objects with different sizes and materials. This often leads to some non-optimal aspect of operation such as read range or directivity. Attempts by some companies have been made to make the tag assembly less expensive.

One such attempt popularised by label converters\(^3\) has been to conductively attach to the antenna an intermediate substrate called a “strap\(^4\)” which has enlarged antenna connections which lead to an RFID chip, rather than attaching the RFID chip directly. This allows the main antenna to be customised for the object to be tagged.

The issues of this procedure are associated with the cost and wastage of the conductive adhesive, the need for tight tolerances on the alignment of the chip to the antenna, the difficulty in handling a (still) small component susceptible to electrostatic discharge (ESD), and the cost in both time and maintenance of temperature curing a conductive adhesive. They are alleviated by coupling the RFID chip to the main antenna via a small loop.

In RFID, different UHF tag antennas are needed to optimise tag performance for different items and different electromagnetic compatibility (EMC) jurisdictions. This is particularly the case for small form factor tags. Product labels are often manufactured for or applied in a particular geographic region to accommodate one or more requirements such as different languages, instructions, or EMC regulations (FCC 2008, ETSI 2009). The two-part design aids in this process.

RFID is today quite commonplace and the growth of the industry has meant a change in the various roles played by the individual manufacturers in getting a tag to its completed form, packagers and label converters are seen to be performing the tag completion.

The two-part design developed by the author enables emerging concepts of tag-on-demand in either ordered batches or smaller label dispensers. One stock keeping unit (SKU), the primary antenna, is required bearing the expensive RFID chip

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\(^3\)A label converter is a company which makes the RFID tag into a peelable sticky label often on a roll for a printer.

\(^4\)A strap is known in RFID as a small substrate which contains a chip which is connected to larger conductive pads so that these larger conductive pads can be glued with conductive glue to another conductive layer which is typically an antenna.
part of the tag and the secondary antenna may be selected or even printed on-demand such that the combination optimises the now completed tag’s read range performance for an EMC jurisdiction, or compensates for the presence of materials surrounding the item. The single common primary antenna offers advantages in volume manufacturing and inventory to both primary antenna supplier and primary antenna applier.

The primary antenna being comparably large with respect to a “strap” actually serves as an advantage in handling and initialisation of the RFID chip.

In the assembly of the completed tag, the two main parts are not in electrical contact but are physically restrained from moving relative to each other by the use of non-conductive adhesive or material, thus a completed tag is not formed until the two-parts are combined.

The secondary antenna may be separate to or may be printed on to or otherwise formed by a product’s packaging as part of that product’s normal manufacturing process. When a primary antenna is glued to the secondary antenna substrate, or sandwiched between a covering layer and the secondary antenna substrate, a specific overlap is required for the two antennas to couple to form a completed tag, however the overlap has relatively loose tolerances when compared to previous RFID chip assembly methods.

The primary antenna is not intended to be removed from the secondary, but if removed the product no longer has RFID capability.

Alternatively, a primary antenna is embedded into a product as part of that product’s normal manufacturing process. An external label containing a secondary antenna is then placed on the product to give the specific overlap required to complete the tag.

### 3.2 Parts of the tag

#### 3.2.1 The primary antenna

The implementation of the antenna comprising the primary antenna is that of a loop antenna. A loop antenna is a good choice for reducing if not eliminating ESD in subsequent stages of the tag manufacture. The primary antenna is formed from a loop antenna made on low-cost substrate with a single conductor layer. Figure 3.1 shows a basic primary antenna. The loop has two sides slanted for marketing aesthetics.
3.2.2 The secondary antenna

The implementation of the secondary antenna is that of a dipole for its ability to maximise the range of the completed tag operating in allowed UHF bands. The secondary antenna conductor may be printed as part of a product’s normal process, or a printed, etched, or an otherwise formed secondary antenna may be affixed to or embedded into part of the product’s components or packaging.

Figure 3.2 shows a simple coupling arrangement to a secondary antenna.

Figure 3.3 shows the secondary with a loop section which increases the coupling between the loop and the secondary antenna, useful for increasing the resistive part of the antenna’s impedance. The regions of the secondary which overlap the inclined edges of the primary antenna were required to be wider than if the primary antenna had rectangular sides both for adequate coupling and allowance for small variations in automated primary antenna placement during assembly.
Figure 3.3. Primary antenna and secondary antenna with alternative coupling.

However, this widened region turned out to be useful to increase the parasitic capacitance between closely coupled tags.

Figure 3.4 illustrates the ability to tailor the tags for use on specific items by changing the secondary design while maintaining a common primary antenna.

3.2.3 The completed tag

The relative positions of the primary antenna and secondary antenna will differ according to their individual form factors, the actual operating radio frequency, and to the material surrounding the completed tag. Further to this, the primary antenna and secondary antenna, which typically would themselves be planar in construction, do not need to be placed in parallel planes or surfaces. For example a completed tag placed at the corner of a carton may have the secondary antenna on
one side and the primary antenna placed on an adjacent orthogonal side such that one edge of the primary antenna still couples to the main edge of the secondary antenna but does so in a three-dimensional fashion.

The tag is not complete until the two main parts are combined. This allows the primary antenna to be placed over a secondary antenna incorporated in a product or packaging at a later stage in a product’s life cycle, and allows the primary antenna to be removed at point of sale for privacy, or the secondary removed for low-range RFID for a return or warranty.

Figure 3.5 shows the basic and minimum elemental layers of the tag. The layers for Figure 3.5 from the top are:

- a protective layer (typically polyester)
- an adhesive layer
- a metal primary antenna conductor and RFID chip
- a PET primary antenna substrate
- an adhesive layer
- a pattern of silver ink
- a paper (or polyester) substrate

Figure 3.5. Elements of the assembly.
Figure 3.6 shows a common alternative for the layers to form a sticky label. Again from the top the layers for Figure 3.6 are:

- a release liner (paper with one side impregnated with a plastic)
- an adhesive layer (large)
- a metal primary antenna conductor and RFID chip
- a PET primary antenna substrate
- an adhesive layer
- a pattern of silver ink
- a paper (or polyester) substrate

The two-part tag design similar to Figure 3.3 looked a good candidate for manipulating the parasitics to work in a close-coupled application as described in Section 2.7 since there are loops available for mutual inductance and the silver ink secondary antenna has wide conductors which could provide mutual capacitance.

A two-part tag design on a 71 mm × 32 mm form factor indeed showed less mutual coupling at small separations than a similar one-part tag, see Figure 3.7, which was qualitatively confirmed with good read-success rates in trials with packed boxes of thin books. Figure 3.8 and Figure 3.9 show the two-part tags with the NXP and Impinj chips respectively. The Impinj chip has less capacitance than the NXP chip; the difference in tuning for the Impinj chip can be seen by the use of a larger loop and an electrically longer secondary dipole antenna.
Figure 3.7. Mutual reactance between pairs of two-part tags.
3.3 Tag testing

Two-part tags with a 71 mm $\times$ 32 mm form factor designed for operation on or in a book were tested using different materials (see Table 2.4) in the form of slabs of dimensions 240 mm $\times$ 125 mm $\times$ 10 mm. The tag design using an NXP chip is shown in Figure 3.8, and the tag design using an Impinj chip is shown in Figure 3.9.

Read ranges and antenna patterns were found using the method of measured minimum power as discussed in Section 2.2. Figure 3.10 shows the read range represented as measured minimum power for a book tag using an NXP chip placed on different materials.

Figure 3.11 shows the read range represented as measured minimum power for a book tag using an Impinj chip placed on different materials.

Figure 3.12 and Figure 3.13 shows the antenna patterns of a book tag using an NXP chip on a 20 mm thick book and a 10 mm thick slab of PTFE respectively.
Figure 3.10. Measured minimum input power for book tag with NXP chip on different materials.

Figure 3.11. Measured minimum input power for book tag with Impinj chip on different materials.
Figure 3.12. Measured E-plane pattern of book tag with NXP chip inside 20 mm thick book. Tag major axis along z-axis, incident field varies with $\theta$.

Figure 3.13. Measured E-plane pattern of book tag with NXP chip on 10 mm thick PTFE. Tag major axis along z-axis, incident field varies with $\theta$. 
3.4 Summary

The two-part tag primarily designed to reduce manufacturing costs allowed flexibility in overall tag design since the secondary antenna part could be integrated into products and could be designed to optimise the coupling between the primary loop antenna and the secondary dipole for a good impedance match to the RFID chip. The designs used for the tagging of books turned out to be broadband for operation in the allowed bands between 850 MHz and 950 MHz. Since the secondary antenna was customised for particular applications the secondary antenna could be adjusted to have differing amounts of inductive or capacitive mutual coupling to surrounding tags, as desired when the files in a stack of files are to be identified. This meant that the tag-to-tag detuning was minimal and a stack of tags could operate with little penalty in read range.
This chapter describes a combined UHF and HF tag. An RFID feature operates at UHF and an EAS feature operates at HF. The antennas of the two features have been designed in such a way as to minimise the interaction between them.
4.1 Introduction

Retail outlets often make use of electronic article surveillance (EAS) tags for deterring shoplifting. Adding an RFID function to an EAS tag may be justified economically if the identification function can offer improved productivity in inventory control such as sales, returns and warranties. In order to minimize interactions between EAS and RFID elements, attempts at combining EAS and RFID functions have placed the EAS element and the RFID element far apart in an end-to-end or side-by-side relationship. This generally leads to an increase in size of the combined tag which is undesirable.

Another method (Checkpoint 2008), shown in Figure 4.1, used in an attempt to keep an existing HF electronic article surveillance tag at the same size, or form factor, has been to allow the addition of a UHF radio identification part to provide some enhancement to an HF part of reduced area so as to gain back some of the performance lost due to that reduction of area. In particular this is done by the addition of a UHF part in the form of a UHF resonant loop which surrounds and couples to the HF part.

4.2 An improved design

If the HF part were allowed to use more area by overlapping the HF and UHF part, the HF part would perform better and would not require any boost by the
layout of the UHF part. Moreover, by surrounding the HF part with the UHF part the UHF part has been constructed in a less than optimal form factor for the UHF part’s operation at UHF. The closed shape used in order to make effectively a single-turn loop resonate with the HF coil is again a loop antenna at UHF, a more open UHF antenna structure, a dipole, has relatively more gain for the space available on a given size tag.

If the HF part were made to overlap the UHF part then we could have a relatively larger HF coil for the available area and we have not compromised the performance of the HF part by adding a UHF part. We can achieve this by using the UHF antenna as connected capacitor plates for two series capacitors to resonate the HF coil. We choose two series capacitors to keep the overall UHF structure symmetrical (dipole). However the main issue in overlapping the HF and UHF parts is uncoupling the HF coil from the UHF part when operating at UHF.

In order to provide the required decoupling, the two connections between the capacitors and the HF coil are made as quarter-wave microstrip lines (at the UHF operating frequency), so although each capacitor is a low impedance at UHF, we effectively isolate the HF part from the UHF part when operating at UHF.

Similarly to Figure 2.5 and the two-part tags described in Chapter 3, the UHF part is laid out as a dipole but the RFID chip is not directly connected, rather it is directly connected to a small loop which is electromagnetically coupled to the dipole, hence the dipole is referred to as a secondary antenna and the small separate loop as a primary antenna. The reason for this separate loop is that the combined EAS and RFID antenna is no more expensive to manufacture than an EAS only antenna, therefore the tag can be used in EAS applications but are “RFID ready” should the user migrate to RFID technology at a later time.

If desired the design can easily be modified (Martin and Hall 2009) to incorporate the RFID chip directly to a single UHF part.

The design is described by figures in the following sections. As is usual with many RFID designs, features of the antenna can be modified on a layer basis during manufacture or could be laser trimmed after manufacture to adjust the operating frequencies of the UHF and HF parts independently.

### 4.3 UHF layer

Figure 4.2 shows the UHF layer, a conductive layer typically one of two sides of an aluminium covered PET supporting substrate. The large C or U shape is a
UHF secondary antenna, a dipole with capacitive ends. These capacitive ends also form one half of the plates of two HF capacitors. In the figure an ellipse highlights a horizontal slot, the length of which can be adjusted for tuning to a different UHF band without influence on the HF part’s operating frequency. The dog-bone shape is the HF coil crossover link which shares this layer. The conductor in the region of the larger ends of this crossover will be later crimped through the substrate to corresponding overlapping regions of the other conductive layer to form a conductive connection.

### 4.4 HF layer

Figure 4.3 shows the HF layer which consists of a coil and two HF capacitor plates, which resonate the coil (a typical frequency used is 8.2 MHz). The larger regions at the central coil’s open ends is where this layer will be crimped to the crossover link on the UHF layer.

### 4.5 Combined UHF and HF layers

Figure 4.4 shows the HF layer on top of the UHF layer. The insulating substrate layer between these two conductive layers is not shown. In the figure an ellipse highlights an area of the HF layer where the capacitor plate is purposely notched.
so the slot in the UHF layer can be trimmed without affecting the overlapping plate area of the capacitor and hence without affecting the HF coil tuning.

It can be seen how the central coil connects to the capacitors via quarter-wave microstrip lines. Each line has a length equal to a quarter wavelength in the substrate material at the UHF operating frequency. In the figure the square highlights a region where the line connection to the top capacitor plate could be adjusted for operation at a different UHF band. Looking into the line from the capacitor end at a UHF operating frequency, this line transforms the coil into a high impedance, so very little current can flow from the top plate of the UHF antenna, through the top HF capacitor, through the coil, through the bottom HF capacitor to the bottom plate of the UHF antenna. Such current through the coil tends to “short out” the ends of the UHF dipole. The quarter-wave lines work to minimise UHF current in the HF layer and hence minimise the impact of the HF coil in close proximity to the UHF antenna.

In the figure a rectangle highlights the constant separation between the lower capacitor plate and the coil. The capacitor plates of the lower layer are larger than the capacitor plates of the top layer, this maintains a constant parasitic capacitance between the lower capacitor plate and the coil and hence a stable UHF antenna tuning even if the top capacitor plate was resized or trimmed to tune the resonant frequency of the HF coil. A suitable separation between conductors of the UHF antenna and the HF coil has been found empirically to be 1 to 2 mm for a tag in

Figure 4.3. The HF layer.
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Figure 4.4. HF layer on top of UHF layer.

air, affixed to one side or sandwiched within a thin cardboard label, affixed to fab-
ric, or affixed to cardboard or plastic packaging. Increasing this separation to 3 to
4 mm is more suitable for encapsulation in thicker cardboard or plastic packaging.

4.6 RFID loop

Figure 4.5 shows the RFID primary loop antenna, which is on its own separate
substrate (not shown) to that of the combined UHF secondary antenna, HF coil
structure.

4.7 The complete tag

Figure 4.6 shows the complete tag with the RFID primary loop antenna on its own
substrate. The primary RFID loop antenna is placed adjacent to the secondary
antenna of the UHF layer, shielding the loop from the isolating lines of the HF coil
layer.

If this tag configuration was used, for example, in a retail application, all products
could have the main part of the tag giving each product an EAS feature; and
the RFID feature could be added, via the attachment of an RFID primary loop
antenna, to high-value products.
Figure 4.5. Separate RFID loop.

Figure 4.6. The complete combined EAS and RFID tag.
Within the stack of layers, starting from the top most layer, there is:

- optional glue and release-liner layers for attachment of the tag to an item;
- HF coil layer;
- main substrate between UHF and HF layers (not shown);
- UHF secondary antenna layer and HF coil crossover link;
- glue (not shown);
- primary RFID loop substrate (not shown); and
- primary RFID loop layer (black) and RFID chip (not shown).

### 4.8 RFID operation of the HF feature

Referring to Figure 4.2, the dog-bone shape HF coil crossover conductor could have a gap cut in it and a chip attached directly to the aluminium conductor across the gap to achieve an RFID function at HF.

In variations of this design a “strap” could be placed across the gap on the UHF layer side, as well as a “strap” could be placed across the coil on the HF layer side.

### 4.9 RFID loop on the UHF layer

Figure 4.7 shows how the primary RFID loop could be merged with the UHF layer for a complete tag containing three layers, two conductive layers separated by an insulating support layer (not shown). Here the primary RFID loop does not overlap the secondary UHF dipole antenna.

### 4.10 RFID loop on the HF layer

Figure 4.8 shows how the primary RFID loop could be merged with the HF layer for a complete tag containing three layers, two conductive layers separated by an insulating layer (not shown). Here also the primary RFID loop does not overlap the secondary dipole (shown in blue).

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Supplementary note:

5A strap is known in RFID as a small substrate which contains a chip which is connected to larger conductive pads so that these larger conductive pads can be glued with conductive glue to another conductive layer which is typically an antenna.
Figure 4.7. The RFID part integrated on the UHF layer.

Figure 4.8. The RFID part integrated in a first way on the HF layer.
Figure 4.9 shows a variation of the RFID loop on the HF layer where the loop overlaps the secondary UHF dipole antenna. The main vertical segment of the UHF dipole antenna has been widened to accommodate the RFID loop conductor and maintain the UHF to HF isolation.

### 4.11 Summary

By designing a UHF dipole which shared the capacitors of an HF tuned circuit, and arranging the connections of the HF coil to the capacitors to form quarter-wave microstrip lines with the UHF dipole, the two antennas were effectively isolated from each other while each antenna could occupy most of the available tag area, thus maximising performance of both UHF and HF features.
THE tag described in this chapter relates to a digital versatile disc (DVD) or compact disc (CD) tag which may be manufactured separately and affixed on to the disc or incorporated within the disc as part of the disc manufacturing process. The antenna designed had minimal radiation in the direction of the disc’s axis. This feature meant a group of closely spaced tagged discs arranged in an on-axis stack as they would be in a retail store had minimal tag-to-tag coupling.
5.1 Introduction

Tags for CDs or DVDs in the market have used HF frequencies with loop antennas. These tags are usually in the form of a sticky label and are affixed on to the disc at the centre within the disc’s data-carrying ring, which in commercial discs is a metal conductor.

The market applications tend towards UHF solutions but the centre of the disc is an environment which is detrimental to the performance of a UHF antenna such as a dipole. Moreover since the disc can be in any particular rotation, even when a dipole at the centre of the disc is well oriented for edge-on reading, the reading performance is poor due to the surrounding metal of the disc.

Discs with UHF dipole tags in their centre are detuned by neighbouring tags when stacked on-axis. The tags which are not at an end position in the stack are also difficult to read face-on due to shielding of the metal of the neighbouring discs. Therefore by using an antenna which promotes reading from the edge-on direction, the tag-to-tag coupling when discs are in a stack is reduced subsequently reducing tag detuning, and there is less shielding due to the neighbouring discs’ metal.

A patch antenna, similarly to the dipole, also suffers from a lack of reading in the edge-on direction. This occurs whether or not the tag is in the metal-free centre region of the disc as the antenna patterns of patch and dipole antennas favour the on-axis direction resulting in tag-to-tag coupling when discs are arranged in an on-axis stack.

A loop antenna in the metal-free region, if electrically small, does have an antenna pattern favouring the edge-on direction, but the surrounding loop of metal of the data-carrying ring interferes with the loop’s performance.

Some discs have a metal layer either within or as an extension to the data-carrying ring which would require any UHF electric dipole or UHF loop antenna at the disc centre to be very small and a poor performer.

By utilising the disc’s data-carrying metal ring as part of a tag’s UHF slot antenna, the limitations imposed by attempting to operate an antenna within a conductive ring are overcome and the tag can be read edge-on. It will be shown later that the tag developed may also be used with discs with only a small conductor-free region in the centre. The tag design is small enough to be applied to the centre of any CD or DVD disc without any change to the disc’s construction or manufacturing process.
5.2 The disc tag antenna

The disc tag’s antenna is constructed as an annular radiating slot in a ground plane, with an additional hole within the metal which is on the inner side of the annular slot so as to accommodate the spindle of the disc player. At operating frequencies in the UHF bands, the annular slot is capacitive and is resonated by adding a serpentine-track inductor across the annular slot, and the resistive part of the matching between the antenna and chip is adjusted by the angular separation between the inductor and the chip feed point. The tuning and feeding of the annular slot is monolithic (in a single conductor plane) which allows the tag to be of a low profile if affixed on to a separately manufactured disc, or incorporated into the data-carrying layer.

Some discs have additional metal in the form of an aesthetic ring within the data-carrying ring making the conductor-free region at the centre small. In the case where there is an annular slot between the data-carrying ring and the additional metal, the annular slot of a stick-on tag antenna is dimensioned such that it overlaps or lies within the disc’s annular slot. If the tag antenna is embedded into the disc, the annular slot of the disc becomes the annular slot of the tag antenna.

In the case where there is no annular slot in the metal of a disc with additional metal, the slot of a stick-on antenna is dimensioned such that the capacitance across the slot is larger than the capacitance between the tag antenna’s inner section, which has been reduced in size, and the disc’s metal. In this case reading is predominately in the hemisphere containing the tag as the disc’s metal shields the tag when trying to read from the face opposite the stick-on tag. If the tag antenna is embedded into the disc with additional metal with no gap between that additional metal and the data-carrying ring, a slot in the disc’s metal would have to be added.

Figure 5.1 shows the basic disc tag developed by the author. The antenna consists of an inner metal ring the ID of which is chosen to be larger than the disc’s spindle hole, an outer metal ring the OD of which is chosen to extend past (or abut to in an embedded tag) the ID of the disc’s data-carrying ring, and a serpentine-track inductor connecting the inner and outer rings. The chip mounting pads extend into the slot between the inner and outer rings such that an RFID chip’s capacitance may parallel resonate the antenna. The concentric rings of the tag effectively produce an antenna pattern similar to an electric monopole along the disc axis above a truncated ground plane, which yields good electric field perpendicular to the edge-on direction.
Figure 5.1. Basic disc tag.

If the tag is to be affixed on to a separately manufactured disc the outside diameter of the outer ring is dimensioned larger than the inside diameter of the disc’s data-carrying ring so as to overlap the disc ring. This overlap is shown in plan view in Figure 5.2, and is also illustrated in Figure 5.3 with the aid of a line coincident with the edge of the disc’s data-carrying ring which line passes through the tag’s outer ring in Figure 5.3. The drawings come from the simulator which uses polygon approximations to circles.

Should the disc itself contain an aesthetic ring, the outer diameter of the tag’s inner ring and the inner diameter of the tag’s outer ring are dimensioned so that the slot in the tag antenna overlaps or lies within the gap between the disc’s aesthetic and data-carrying rings, or in the case where there is no gap the slot is reduced in width and the inner metal surround is changed such that the capacitance across the slot is larger than the capacitance between the tag antenna’s inner ring and the disc’s ring layer.

If the tag is to be incorporated into the disc’s manufacturing process the outside diameter of the outer ring is dimensioned equal to the inside diameter of the disc’s data-carrying ring so as to contact the disc ring. Should the disc itself contain an aesthetic ring, the outer diameter of the tag’s inner ring and the inner diameter of the tag’s outer ring are dimensioned so that the slot in the tag antenna corresponds to or lies within the gap between the disc’s aesthetic and data-carrying rings and the tuning inductor is added, or in the case where there is normally no gap both an annular slot and a tuning inductor are introduced to the disc’s single ring layer.
Figure 5.2. Tag on disc. The different coloured region inside the grey is the region of overlap.

Figure 5.4 shows two discs on axis as typically found when the discs are stored or displayed on a shelf, with the edge-on direction being the direction typically required for reading and the direction for which other solutions have weak reading.

Figure 5.5 shows the basic layers involved in the case where the tag is manufactured separately from the disc. The layer thicknesses are exaggerated for clarity. The line CL indicates the centre line axis of the disc and tag. The edge IDd indicates the inner diameter of the disc’s spindle hole and the edge IDt indicates the inner diameter the tag’s hole should have so as not to interfere with a storage or a play spindle. Layer PC represents a first disc substrate layer. Layer DC represents the disc’s data-carrying layer of a compact disc or the combined data-carrying layers and intermediate adhesive layer of a digital versatile disc. The edge IDdc indicates the inner diameter of the disc data-carrying layer(s) and may be closer to edge IDd for the case of a disc containing an aesthetic ring. Layer PC/INK indicates a second disc substrate of a digital versatile disc or a decorative ink/protective layer of a compact disc. Layer GLUE indicates and adhesive layer between the disc and the tag substrate PET. Layer IR is the tag antenna inner
Figure 5.3. Alignment of disc and tag.

Figure 5.4. Two discs on axis.
ring separated by slot S to the tag antenna outer ring OR. It should also be noticed that tag outer ring inner diameter is less than edge IDdc, and tag outer ring is greater than edge IDdc for the case of a disc without an aesthetic ring, in which case layer S/A/A may be substrate material, adhesive, air, or a combination of such. In the case where the disc has an aesthetic layer, region S/A/A will be reduced as edge IDdc would be closer to edge IDd, and layer DC may or may not have a slot with such slot if present typically being in the vicinity of edge IDdc as shown. For the aesthetic layer case the capacitance between IR and OR across S is chosen to be larger than the capacitance between IR and DC. The region above layers PET, IR and OR may contain an adhesive and protective film or a protective coating above the tag. The chip is connected across S and a serpentine-track tuning inductor formed between IR and OR.

Figure 5.6 shows the basic layers involved in the case where the tag is manufactured as part of the disc. The layer thicknesses are exaggerated for clarity. The line CL indicates the centre line axis of the disc. The edge IDd indicates the inner diameter of the disc’s spindle hole. Layer PC represents a first disc substrate layer. Layer DC represents the disc’s data-carrying layer of a compact disc or the combined data-carrying layers and intermediate adhesive layer of a digital versatile disc. Layer IR is the tag antenna inner ring separated by slot S to the tag antenna outer ring OR. In some discs layer OR is not present, the slot S being between the data-carrying layer DC and inner ring IR. In discs where an aesthetic ring is present, that ring would be layers IR and OR, with slot S formed in the aesthetic ring as a modification. Layer PC/INK indicates a second disc substrate
of a digital versatile disc or a decorative ink/protective layer of a compact disc. Layer S/A/A may be substrate material, adhesive, air, or a combination of such. The chip is connected across S and a serpentine-track tuning inductor formed between IR and OR.

Figure 5.7 shows the E-plane field pattern of the separately manufactured or stick-on tag without a disc aesthetic ring, or the tag manufactured as part of the disc. This radiation pattern is also valid for an embedded tag with or without the extra metal of the aesthetic ring.
Figure 5.8. E-plane radiation pattern of a stick-on disc tag with extra metal in the centre of the disc.

For the case of a separately manufactured or stick-on tag with a disc aesthetic ring, the radiation is predominately in the “top” hemisphere which is closest to the printing on the disc as shown in Figure 5.8. This is because the tag is mounted on the top of the disc closer to the side with the printing, and the disc data-carrying layer and the additional metal of the aesthetic ring (which reduces the metal-free region at the disc centre) form a ground plane under the tag’s radiating slot reducing the radiation in the “bottom” hemisphere.

In all tag cases, there is no field on axis which reduces tag-to-tag coupling in an on-axis stack, but enough field at small angles off axis to enable tag reading with a passing reader antenna such as a handheld antenna or wand antenna in applications where the discs are displayed front-on.

5.3 Testing the tag

An EPC Global industry demonstration required that DVDs in cases be placed on a metal shelf in 40 adjacent slots each of dimensions 0.15 m × 0.30 m × 0.30 m with no barrier between slots, with 12 DVDs per slot oriented face-on for display to a retail customer, and a required read range of 0.3 m from a handheld reader. Figure 5.9 shows the arrangement, only 5 slots of 12 DVDs each are shown for clarity.

All the tags were successfully read even though the antenna does not have any E-plane field on the axis of the disc. The facts that the tags had little on-axis coupling
to neighbouring tags in a slot and the handheld reader swept across the disc’s face so as to explore fields in non-axis directions allowed successful tag-to-reader coupling.

### 5.4 Summary

A tag antenna for a CD or DVD was designed utilising the metal that already exists in the discs. Two variants were designed, one to be stuck on to existing products, and a second which could be integrated into the disc during manufacture. A stick-on tag was formed using 18 µm Al on 50 µm PET and an Impinj Monza2 chip, 480 such tags placed on standard DVDs in cases on a metal shelf were successfully demonstrated at a read range of 0.3 m in an EPC Global industry demonstration.
This chapter describes a matching technique to obtain useful range from electrically small UHF loop antennas. For reasons such as production cost, external matching components are not used but are rather integrated into the antenna using the conductors and associated supporting substrate.
6.1 Introduction

The extent of reflection (\(\Gamma\)) that takes place at an interface between the antenna and the associated circuit is represented by the following expression:

\[
\Gamma = \frac{Z_{\text{chip}} - Z_{\text{ant}}}{Z_{\text{chip}} + Z_{\text{ant}}}
\]

The transmission factor representing the level of power that passes the interface is defined as \(1 - |\Gamma|^2\). A transmission factor of unity denotes that all available power from the antenna is transferred to the associated circuit. Although unity represents an idealised lossless case, factors close to unity are achievable in practice. This chapter will describe an integrated matching method that achieves this objective.

6.2 A small UHF loop

In a UHF passive circuit that requires rectification of the reader carrier, the input impedance may typically be capacitive, for example 20 - j200 Ω. For maximum power transfer the associated antenna should exhibit an inductive reactance 20 + j200 Ω. In order for an electric UHF antenna to exhibit an inductive reactance of j200 Ω, the physical dimensions of the antenna should be close to \(\lambda/2\) in length, or by using common shortening techniques around \(\lambda/4\) in length. Antennas shorter than this will have a radiation resistance less than the circuit resistance and will have a capacitive reactance requiring matching. Sadiku (Sadiku 1989a) gives the radiation resistance for a small square loop of area \(S = d^2\) and maximum dimension \(d \leq \lambda/10\) as:

\[
R_{\text{rad}} = \frac{320\pi^4 S^2}{\lambda^4}
\]

Sadiku (Sadiku 1989b) also shows that the magnetic field in the centre of a filamentary circular loop of radius \(r\) is the same for a regular polygon with \(n\) sides which circumscribes the circle of radius \(r\) and carries the same current \(I\):

\[
H_{\text{centre}} = \frac{nI}{(2\pi r)} \sin\left(\frac{\pi}{n}\right)
\]

Since for a small loop we can approximate the current as uniform (Ramo et al. 1984), we can get an idea of the inductance of a square loop from the inductance of a filamentary circular loop (Sadiku 1989c) of radius \(\rho_0\) and wire diameter \(d_w\)
Figure 6.1. Loop antenna with no matching.

The equivalent diameter of a track is covered in Section 2.5) having the same area 
\[ S = d^2 = \pi \rho_0^2 \]

\[ L = \frac{\mu_0 l}{2\pi} \left[ \ln \left( \frac{4l}{d_w} \right) - 2.45 \right] \quad l = 2\pi \rho_0 \quad \rho_0 \gg d_w \]

In order for a single-turn UHF loop antenna to exhibit an inductive reactance of 
\( j200 \, \Omega \) at 915 MHz, the physical dimensions of the antenna should be around 
\( \lambda/25 \). A loop of this size is electrically small and has a radiation resistance much 
smaller than the RFID circuit’s equivalent series resistance. Antennas larger than 
this will have an increased radiation resistance but will also have an increased 
inductance which is too high to simply be resonated by the chip’s capacitance. 
Loops larger than that for simple resonance with a chip require that both real and 
imaginary parts of the antenna impedance be matched to the chip.

While a good match is preferred, when small antennas are used the components 
required for matching can be similar in size to the antenna itself, which if not 
integrated will combine to form a combined antenna and matching network that is 
larger in size to that intended, placing into question the original choice of antenna. 
A slightly larger antenna without matching might perform sufficiently.

Figure 6.1 shows a loop antenna with no matching, the loop is simply made as 
large as the overall tag form factor allows, and the internal area sized such that 
its inductance resonates with the chip capacitance. This results in an equivalent 
current path around a loop smaller than the tag area.
Figure 6.2. Loop antenna with an increased equivalent current path.

Figure 6.3. Equivalent circuit of a loop antenna matching network.

Figure 6.2 shows a loop antenna making better use of the available tag area. This results in a loop with an increased current path radius and therefore better radiation characteristics, but the inductance of the loop is too large to resonate the chip.

Figure 6.3 shows an equivalent circuit of a loop antenna matching network at 915 MHz. The antenna is represented as an impedance of $2 + j400 \, \Omega$, a resistive part lower than 20 $\Omega$, and an imaginary part more inductive than the $j200 \, \Omega$ of our example chip. There are two typical two-element matching networks; the one chosen avoids the use of an inductor since we wish to have our inductor antenna use as much of the tag area as possible.
Figure 6.4 shows the intermediate points of our matching network on a 50 $\Omega$ Smith chart as we move from the antenna resistance and combined inductance to the chip equivalent series resistance, with the last step using the chip equivalent series capacitance. The network evolves by first adding in some series capacitance to reduce the inductive reactance resulting from our overly large loop; secondly we add some shunt capacitance which bumps up the real and imaginary parts of the impedance; and thirdly we move through the chip’s equivalent series capacitance to match to our final 20 $\Omega$ target.

Figure 6.5 shows a large loop antenna formed from the conducting layer on the first side of a supporting substrate with the matching-network elements added via a second conductive layer on the second side of the substrate. A cut opposite the notched-gap chip location forms a series capacitor with a plate on the second conductive layer, and a further plate under the chip location forms the shunt capacitance.

If the matching condition is required to produce a particular operating bandwidth, then a similar technique may be used except that the resistive part of the antenna may be transformed by the matching network to a magnitude other than the equivalent series resistance of the chip circuit. By using the value of the
chip circuit’s equivalent parallel resistance $R_{\text{chip}}$ as the resistance to which the antenna’s equivalent series resistance $r_{\text{ant}}$ is transformed, the bandwidth may be found by taking the relation:

$$(Q^2 + 1)r_{\text{ant}} = R_{\text{chip}}$$

with $Q = \frac{f_c}{BW} > 0$ so that $r_{\text{ant}} \neq R_{\text{chip}}$

where $BW$ is the bandwidth and $f_c$ the centre frequency. This is rearranged to give:

$$BW = \frac{f_c}{\sqrt{\frac{R_{\text{chip}}}{r_{\text{ant}}} - 1}}$$

Equation 6.1 is a useful first-order approximation when relatively large bandwidths are desired, such as those currently required for an international UHF tag (865 to 956 MHz).

### 6.3 Testing the integrated matching network

A 19 mm $\times$ 19 mm loop of track width 1 mm was made with double sided 37 $\mu$m Cu on a 0.36 mm FR4 substrate for a livestock application. Read range was around
1.5 m using an Alien EPC Class-1 chip. This range was suitable for a tag worn on the ear of an animal, the tag reading when passing under a circularly polarised reader antenna, as the loop axis would be mostly parallel with the ground as it dangled from the animal’s ear. A loop similar to Figure 6.1, having the same outer dimension but wider 6 mm tracks so that it directly resonated with the chip barely reached 1 m range in ideal laboratory conditions.

### 6.4 Summary

Small loops can be made larger than the size dictated for simple resonance with the chip capacitance by making a matching network which is integrated into the antenna itself. The larger loop benefits from having a larger radiation resistance, and a better impedance match to an RFID chip resulting in a larger operating bandwidth.
TAGGING metallic objects is always a challenge since the boundary conditions of a plane wave incident on a metal surface require the electric field to reduce to near zero. A 2 mm thick piece of ferrite impregnated rubber was used between a tag and a metal surface in order to operate a tag with only a 2 dB penalty in received power while still being relatively low profile against the metal surface. Some original methods of measurement of the surface impedance of the material when it is backed by metal are described.
Chapter 7  Increasing the UHF Field Near Metal

7.1  Introduction

At the planar interface between two media, the boundary conditions for wave propagation at normal incidence from medium_1 to medium_2 give the following result for the reflection coefficient:

\[ \Gamma = \frac{E_{ro}}{E_{io}} = \frac{\eta_2 - \eta_1}{\eta_2 + \eta_1} \]  \hspace{1cm} (7.1)

where

\[ \eta = \sqrt{\frac{\mu}{\epsilon}} \]

and \( E_{io} \) and \( E_{ro} \) are the tangential incident and reflected fields at the interface.

The complex forms of both the permeability and the permittivity are given by \( \mu = \mu' - j\mu'' \) H/m and \( \epsilon = \epsilon' - j\epsilon'' \) F/m. The resulting electric field \( E_s \) in medium_1 at the interface is:

\[ E_s = E_{ro} + E_{io} \]

When a plane wave in air (medium_1 \( \eta = \eta_0 = 377 \) ohms) is incident on a metal surface (medium_2 \( \eta \approx 0 \)) \( \Gamma = -1 \), so the electric field \( E_s \) is zero at the boundary. It increases sinusoidally in magnitude as we traverse in the air back from the interface reaching a maximum of twice the incident field at a quarter of a wavelength away (\( \approx 82 \) mm away from the metal interface at 915 MHz). A dipole antenna placed a small distance of say 2 mm away from a metal surface therefore receives only a small electric field.

A library application involving the movement of archive film material required the tagging of the metallic storage canisters which measured 280 mm in diameter and 42 mm thick.

7.2  Electromagnetic absorber material

Investigations into non-reflective coatings for electromagnetic shielding of mobile phones (Min et al. 2008) have noted that materials with magnetic and dielectric losses can be used on a metal surface to reduce the reflection from the metal. For the case of RFID tags, if such material is placed on a metal surface with the tag placed on the absorber (with the tag antenna conductor insulated from the conduction of the absorber) less reflection from the “coated” metal means more of the incident field is available for tag operation near to the metal surface.
From reading brochures on such material, the influence of the absorber material parameters with thickness on the actual amount of absorption was unclear so the following derives such an expression.

Using transmission line theory, the impedance seen at the air-to-absorber interface of the absorber backed by metal can be found using the following:

\[
Z_{\text{in}} = Z_{\text{absorber}} \left[ \frac{Z_L + Z_{\text{absorber}} \tanh (\gamma l)}{Z_{\text{absorber}} + Z_L \tanh (\gamma l)} \right]
\]

with \( Z_L = 0 \) for the metal, and \( Z_{\text{absorber}} = \eta_{\text{absorber}} = \sqrt{\mu/\epsilon} \) for the absorber of thickness \( l \), the impedance at the air-to-absorber interface normalised to \( \eta_0 = \sqrt{\mu_0/\epsilon_0} \) in free space is:

\[
z = \frac{Z_{\text{in}}}{Z_0} = \frac{\eta_{\text{in}}}{\eta_0} = \sqrt{\frac{\mu_r}{\epsilon_r}} \tanh (\gamma l)
\]

Since we are using the complex permeability and permittivity, from the wave-equation solution we seek a propagation constant \( \gamma \) where:

\[
\gamma^2 = -\omega^2 \mu \epsilon
\]

so \( \gamma \) is:

\[
\gamma = j \omega \sqrt{\mu \epsilon}
\]

An absorbing material was investigated theoretically using the properties from the aforementioned mobile-phone absorber at 900 MHz which were read graphically as \( \mu_r = 5.3, \mu''_r = 6, \epsilon'_r = 125, \) and \( \epsilon''_r = 12 \).

Writing in a form to use these quantities:

\[
\gamma = j \omega \sqrt{\mu \epsilon} = j \frac{\omega}{c} \sqrt{\mu_r \epsilon_r}
\]

where \( c = 1/\sqrt{\mu_0 \epsilon_0} \) is the velocity of light in a vacuum, so:

\[
\gamma = j \frac{\omega}{c} \sqrt{\mu_r \epsilon_r} = j \frac{2\pi}{\lambda_0} \sqrt{\mu_r \epsilon_r}
\]

and

\[
z = \frac{\eta_{\text{absorber on metal}}}{\eta_0} = \sqrt{\frac{\mu_r}{\epsilon_r}} \tanh \left( j \frac{2\pi l}{\lambda_0} \sqrt{\mu_r \epsilon_r} \right) \quad (7.2)
\]

We can see in Equation 7.2 that the product of the relative values of permeability and permittivity acts to effectively reduce the wavelength in the material from the free-space wavelength \( \lambda_0 \), so that a physically thin piece of material effectively moves the antenna further from the metal surface.
Substituting $\eta_{\text{absorber, on metal}}$ for $\eta_2$ in Equation 7.1 gives a reflection coefficient for air to the combined absorber-on-metal structure.

The amount of reflection in dB can be calculated as the return loss:

$$\text{ReturnLoss} = -20 \log |\Gamma|$$

Figure 7.1 shows the return loss for thickness of the material around 2 mm at 850 MHz, 900 MHz, and 950 MHz. It can be seen that the reflected wave is attenuated by around 6 dB.

### 7.3 Designing a tag for a metal surface

The sample material described in Section 7.2 was used in simulation for 2 mm of absorber material placed on the side of a cylindrical metal film canister, of diameter 278 mm and height 42 mm, with a dipole tag separated by 1.5 mm thick foam tape and the dipole length aligned along the circumference. The film canister was approximated as a plane of metal (copper) of size 42 mm × 278 mm.
Figure 7.2 shows the impedance of the tag antenna at 915 MHz in free space, when its length is varied. As expected the tag is resonant when its length is a little shorter than 154 mm (0.47\(\lambda\)).

Figure 7.3 shows the impedance of the tag antenna near finite-sized metal and near an infinite ground plane to see the effect of the finite-sized metal used to model the film canister. The resonant length was shifted to above the one half wavelength seen for free space. In the modelling a distance of 3.5 mm above the metal was used as it was intended to use 2 mm of absorbing material and a 1.5 mm foam spacer between the tag and the absorber.

Figure 7.4 shows the impedance of the tag antenna placed on 1.5 mm of foam which is placed on a piece of absorbing material with parameters drawn from Section 7.2 of cross section 8 mm \(\times\) 100 mm and thickness 2 mm. The antenna was resonant with a length around 96 mm.

### 7.4 Fabricating a tag for a metal surface

A product called Eccopad\(^6\) type UHF-G2 consists of a 2 mm thick absorber material and a 0.5 mm thick foam insulator. The material details (an industry secret) were not available but the absorber was stated as being a ferrite powder suspended in a silicon rubber, sometimes referred to as carbonyl-iron rubber.

The two-part tag antenna which was simulated in Figure 7.4 was fabricated with a slab of the Eccopad material 8 mm \(\times\) 100 mm of 2 mm thick material, and 1.5 mm of foam insulation. The empirical length of the secondary dipole for best read range on the film canister was found to be 84 mm. Considering the resonance of the simulated tag above metal required a length of around 96 mm the Eccopad material seemed to be a more effective absorber than the mobile-phone absorber since we can see from Figure 7.3 that the presence of metal pushes the resonant length longer, and the greater the reduction in resonant length the more effective the absorber is in removing the effect of the metal.

Figure 7.5 shows the plan view of the tag.

Figure 7.6 shows the layers of the tag (layers not to scale).

The read range was 2.16 m using the 902 to 928 MHz FCC band at an EIRP of 36 dBm. This was suitable for a standard doorway width antenna (array) to track movement of film canisters.

\(^6\)Made by Emerson & Cuming.
Figure 7.2. Tag antenna impedance at 915 MHz in free space.
Figure 7.3. Tag antenna impedance at 915 MHz 3.5 mm above metal.
Figure 7.4. Tag antenna impedance at 915 MHz when spaced 1.5 mm above 2 mm of absorber mounted on metal.
Measurements on the absorber material

The Eccopad material was tested at a frequency of 909.1 MHz in a 550 mm air-dielectric slotted coaxial line of $D_{\text{inner}} = 6.2 \text{ mm}$, $D_{\text{outer}} = 14.2 \text{ mm}$, and $Z_0 = 50 \Omega$ by inserting a 2 mm thickness into the end of a short circuit. The scale of the slotted line measured relative distances from the source.

Before insertion of the material, observations of the short circuit gave a VSWR of 100 (40 dB) and voltage minima at 301 mm and 466 mm and hence a $\lambda = 330 \text{ mm}$ (909.1 MHz).
When the 2 mm thickness of the material was placed into the short circuit, the VSWR changed to 13.49 (22.6 dB) and the position of the voltage minimum moved to 486.5 mm i.e. 20.5 mm further away from the source. At the new $V_{\text{min}}$, $z_L = 1/V_{\text{SWR}} = 0.0741 + j0$. To find the impedance at the front face of the inserted material we transfer this value through a distance of 486.5 - 466 + 2 = 22.5 mm away from the load, which is $(22.5/330)\lambda = 0.0682\lambda$. Using:

$$z_{\text{in}} = \frac{z_L + j \tan \left( \frac{2\pi l}{\lambda} \right)}{1 + jz_L \tan \left( \frac{2\pi l}{\lambda} \right)}$$

we get a normalised impedance $z_{\text{in}}$ of $0.0895 + j0.4537$. The reflection coefficient can then be calculated using:

$$\Gamma_{\text{in}} = \frac{z_{\text{in}} - 1}{z_{\text{in}} + 1}$$

to yield $\Gamma_{\text{in}} = -0.5645 + j0.6515 = 0.8620 \angle 131^\circ$. To find the fraction of the electric field at the surface of the material we use:

$$|1 + \Gamma_{\text{in}}| = |0.4355 + j0.6515| = 0.7836$$

We therefore have around 78% of the incident field left at the material surface to energise a tag.

Without the material, at a position 2 mm from the short circuit the normalised impedances $z_L$ of $0.0100 + j0$ and $z_{\text{in}}$ of $0.0100 + j0.0381$ were calculated from the VSWR of 100. This gives a $\Gamma_{\text{in}}$ of $-0.9774 + j0.0746$ and $|1 + \Gamma_{\text{in}}| = |0.0226 + j0.0746| = 0.0779$, so 7.8% of the incident field exists at that position.

Therefore at the 2 mm position from the metal surface we have through the use of the absorbing material increased the available field from around 7.8% to around 78%, quite a considerable increase in field for a 2 mm thickness of material. This value of 78% is only 2 dB lower than the full incident field value of 100%.

In order to achieve this amount of remaining field without any absorber material we can calculate the distance $l$ of the tag from the metal surface by using the relation:

$$|E_{\text{total}}| = 2|E_i| \sin \left( \frac{2\pi l}{\lambda} \right)$$

Rearranging for the distance $l$ from the metal surface:

$$l = \frac{\lambda}{2\pi} \arcsin \left( \frac{|E_{\text{total}}|}{2|E_i|} \right)$$

For $\lambda = 330$ mm and $|E_{\text{total}}|/|E_i| = 0.7836$ we get a value for $l$ of 21.14 mm.
Thus the absorber material allows for a much lower profile tag when required to be mounted on a metal surface.

7.6 Summary

Using a 2 mm thick piece of absorbing material, of the type whose properties were measured in Section 7.5, of size 8 mm × 100 mm, on a metal surface the field available for tag operation increased from 7.8 % to 78 %. To achieve 78 % of remaining field without absorbing material would require the tag to be placed at 21.14 mm from the metal surface (at 909.1 MHz).
Chapter 8

A Drill String Identification Tag

In this chapter the problem of getting magnetic field down to the bottom of a metal well, as may be required in applying RFID technology to drilling strings in oil exploration, is studied. The performance of a successful design has been verified in a practical application. Extensive measurement of ambient noise, which was thought might have, but did not in fact impede successful operation, are reported.
8.1 Introduction

A tag is to be placed into a hole drilled into a mining drill string, specifically in the screw-coupling region where the material thickness is over-engineered, and could take a nominal 25.4 mm diameter hole around 25.4 mm deep. In operation the drill string contacts and wears against the surrounding earth and experiences up to 6.35 mm reduction in radius, thus the hole depth will reduce by this amount in service. It is desired to develop and test a suitable RFID tag for this application and to confirm its operation will survive this wear and will not be defeated by the presence of the environmental noise found in the application.

8.2 Construction of the test well

A ferrite-cored solenoid coil seemed to make sense for a coil located against a metal surface, the metal surface parallel to the coil axis aids the magnetic field in the coil. The question was could a magnetic excitation field at 13.56 MHz penetrate far enough into the hole for useful coupling to the tag?

A U-shaped core was chosen, as it would allow the coil and electronics to sit safely below the surface and the “legs” of the core would direct magnetic field down through the coil. Ferrite sections were available for testing, cross section 8 mm × 13.85 mm, length 7.5 mm, and the material was Neosid F25 which at 13.56 MHz has parameters $\epsilon_r = 12$, $\mu_r = 50$, bulk conductivity 0.001 S/m, and a tanδ = 0.005 (magnetic). These sections were glued closely together and rectangular U-shaped cores made with leg length differences of 7.5 mm to simulate the wearing. Production cores would likely be potted in drilled holes with an epoxy material so the well would likely be circular. A rectangular well could be formed within a cylindrical plug to be pressed into the circular drilled hole. In any case, for convenience of locating coils in a well for testing, a rectangular cross section for the well was chosen.

Two wells were machined from brass, both 25.4 mm × 17.5 mm in cross section with one 18 mm deep and the other 25.5 mm deep, a 7.5 mm difference to suit the available ferrites and more than the expected amount of wearing.

Figure 8.1 shows a photograph of the deep well.

The coil axis would be placed parallel to the excitation magnetic field and to obtain the longest solenoid this corresponded to the long dimension of the well cross section. If we designate this as waveguide dimension $a$, then the orientation of
magnetic field is consistent with the TE$_{10}$ mode ($a$ along $x$, $b$ along $y$, and propagation into the well along $z$). This choice of direction is also consistent with the electric field existing across the smallest cross section dimension.

Assuming lossless walls, the attenuation constant for the TE$_{10}$ mode for the well dimensions at 13.56 MHz is as follows.

\[
\gamma = \sqrt{\left( \frac{m\pi}{a} \right)^2 + \left( \frac{n\pi}{b} \right)^2 - k^2}
\]

where \(k^2 = \omega^2 \mu \varepsilon \approx 0.0808 \text{ m}^{-2}\)

\[
\gamma = \sqrt{\left( \frac{\pi}{25.4 \times 10^{-3}} \right)^2 - 0.0808} = 123.6844 \text{ m}^{-1}
\]

So since \(\gamma\) is real with lossless walls assumed, the well is a waveguide beyond cut-off with an attenuation constant of \(\alpha = 123.6844 \text{ Np/m}\).

A difference of 7.5 mm in the $z$ direction is a field attenuation of:

\[
e^{-123.6844 \times 7.5e^{-3}} = 0.3955
\]

\[
20 \log(0.3955) = -8.06 \text{ dB} \tag{8.1}
\]

so 8.06 dB is the attenuation along a 7.5 mm depth of this well.
The attenuation constant for a TE\textsubscript{01} mode with lossless walls is calculated for comparison.

\[ \gamma = \sqrt{\left(\frac{\pi}{17.5 \times 10^{-3}}\right)^2 - 0.0808} = 179.5194 \text{ m}^{-1} \]

Therefore \(\alpha = 179.5194 \text{ Np/m} \).

The attenuation for 7.5 mm is 11.69 dB, more than for the TE\textsubscript{10} mode which shows that propagation favours an orientation where the electric field exists across the smallest cross section dimension.

### 8.3 Construction of a drill string model

An octagonal aluminium box was constructed to house the test well and approximate a circular 6 inch diameter drill string (the octagon had an inscribed circle diameter of 150 mm), the well being on one of the octagon sides. The octagonal box was made with a removable cover which allowed access to the base of the test well to change coil cores and well depths. A small fifty ohm cable linked the test well to a BNC bulkhead connector in the fixed cover. The cable connecting the coil to any measuring apparatus was shielded from the exciting magnetic field, exiting the box from the base so as to run parallel with the field keeping induced currents to a minimum. A photograph of this assembly appears in Figure 8.2.
8.4 **Construction of test coils**

Two initial test coils were made by winding three turns of 1.5 mm wide copper tape (t = 75 µm) around ferrite cores. One end of a coil was connected to the centre conductor of an SMA panel-mount connector, the other soldered directly to the removable base of the test well.

8.4.1 **Impedance inside the well**

The testing apparatus was placed on a perspex sheet mounted on wooden legs, and connected to a HP 8752A network analyser. At the end of the 50 Ω cable connected to the test well, a shorted SMA connector allowed a reference plane to be set at the coil location. The inductance at 13.56 MHz for the coil without legs was 174.73 nH ($r_s = 1.5029 \, \Omega$) and with legs was 433.47 nH ($r_s = 1.9902 \, \Omega$), the legs increasing the inductance by a factor of 2.48.

8.4.2 **Calculation of source voltage from coils**

When the coils were directly connected to the fifty ohm input of a spectrum analyser as is shown in Figure 8.3, since the two coils have different inductances and therefore different source voltages, it is really the available source powers not the delivered powers into a load that must be compared.

It was decided that the coil should be brought to parallel resonance, so the dynamic impedance was better positioned on the Smith chart for accurate reading, and the quality factor of the coil could be more accurately determined. The three-turn coil with legs had a parallel-resonant dynamic impedance of 1.17 kΩ and therefore a large reflection coefficient. A reflection coefficient of less than one half
Figure 8.4. Single-turn test coils and some calibration short circuits.

is desired so that the correction factor to the spectrum analyser’s received power is not too large.

Both coils were modified to a single turn of 6 mm wide copper tape (t = 75 µm). The coils were brought to resonance by the addition of shunt capacitance. A photograph of both coils, and the short circuits used, is shown in Figure 8.4.

The impedance of the coil without legs in the deep well is shown in Figure 8.5, and the impedance with parallel resonance with a capacitor placed close to the back of the well is shown in Figure 8.6.

Using the dynamic impedance from Figure 8.6, the voltage reflection factor at resonance for the coil without legs was:

\[ \Gamma = \frac{Z_1 - Z_0}{Z_1 + Z_0} = 0.326 \]

This implies that 10.6 % of the power was reflected and the received-power correction factor to obtain the available source power was 1.119 (0.49 dB).

The impedance of the coil with legs in the deep well shown in Figure 8.7, and the impedance with parallel resonance with a capacitor placed close to the back of the well is shown in Figure 8.8.

Using the dynamic impedance from Figure 8.8, the voltage reflection factor for the coil with legs was:

\[ \Gamma = \frac{Z_1 - Z_0}{Z_1 + Z_0} = 0.507 \]
Figure 8.5. Impedance of test coil without legs in deep well.

Figure 8.6. Dynamic impedance of test coil without legs in deep well.
This implies that 25.7% of the power was reflected and the received-power correction factor to obtain the available source power was 1.346 (1.29 dB).

### 8.4.3 Power from coil in a magnetic field

A square loop antenna with inside dimension of 300 mm × 300 mm was used for the magnetic field creation. This antenna had been previously characterised and was well-matched to 50 Ω with a $Q \approx 1$, so no significant field variation would occur for small tuning variations around 13.56 MHz. This loop antenna was excited with 1 W at 13.56 MHz.

### 8.5 Available source power

The test apparatus was placed in the centre of the excitation antenna, with the coil connected to a HP 8594E spectrum analyser. The drill string model was first arranged with the test-well edge parallel with the excitation-antenna edge as shown in Figure 8.9.

Table 8.1 shows the data recorded with the drill string model placed in two positions, one with the test-well edge parallel with the excitation-antenna edge, and
Figure 8.8. Dynamic impedance of test coil with legs in deep well.

Figure 8.9. Drill string model in square loop antenna.
the other where the well axis points to the antenna corner. Input to the excitation antenna was 1 W, which yielded an average magnetic field across the well face of 829 mA/m. The reflection factor between the test coil and the spectrum analyser was taken into account so the available source power of the coil was calculated as $P_{\text{corrected}}$.

An increase in available source power of 16.5 dB for the addition of legs was indeed worthwhile since from Equation 8.1 we expect -8.06 dB attenuation for every 7.5 mm of hole depth. However even with the improvement, the absolute power of -12.7 dBm was too low for the ISD 6408 chip which requires -2.5 dBm for robust operation (when the subcarrier oscillator is 200 kHz).

A HP 11941A close-field probe was placed on the excitation-antenna mounting surface against the test-well edge and oriented for maximum coupling of magnetic field. The drill sting model had the cable to the spectrum analyser removed and a fifty ohm termination connected in place. The spectrum analyser recorded a voltage of 80.12 dB$\mu$V at edge position and 80.05 dB$\mu$V in corner position. The probe has an interpolated antenna factor of 38.12 dB$\mu$A/m/$\mu$V and cable loss was 0.17 dB (3110 mm length). The magnetic field was 832.7 mA/m (edge) and 826.0 mA/m (corner). A familiar HF tag with a form factor a little smaller or similar to a credit card is fully operating at around 120 mA/m, so the magnetic field from the small low-Q-factor antenna with 1 W was not too far away from a typical HF operating scenario, so more power and a higher-Q-factor antenna looked to be sufficient for tag operation.

Experimentation has led to the conclusions that 10 W of input power in a 50 $\Omega$ system is about the limit from a receiver noise aspect without requiring extraneous filtering, and a Q factor of 20 is about the limit in regards to detuning by human
or metallic object movement. Due to the nature of the conditions on an oil drilling rig it was decided to limit the antenna Q factor to 10.

8.6 On-site noise measurements

Measurements of noise from a drilling rig at Moomba South Australia were taken to see to what extent the environmental and man-made noise under the platform of a drilling rig would have on an HF RFID system. It is intended that a drill string tag shall reply at a frequency of 13.56 MHz.

8.6.1 Equipment used

An HP 8594E spectrum analyser was connected to an EMCO 6507 active receiving loop antenna which was suspended below the platform of the rig. Figure 8.10 shows the receiver antenna below the platform and adjacent to the bell nipple, a position which reasonably simulates that of a proposed reader receiver antenna.

The appropriate active-loop antenna factors for the bands under investigation are summarised in Table 8.2.
Table 8.2. Receiving antenna factors.

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Antenna Factor (dBµA/m/µV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.075</td>
<td>-33.9</td>
</tr>
<tr>
<td>0.100</td>
<td>-34.4</td>
</tr>
<tr>
<td>0.150</td>
<td>-34.7</td>
</tr>
<tr>
<td>0.250</td>
<td>-34.7</td>
</tr>
<tr>
<td>1.000</td>
<td>-34.9</td>
</tr>
<tr>
<td>2.000</td>
<td>-34.2</td>
</tr>
<tr>
<td>5.000</td>
<td>-34.3</td>
</tr>
<tr>
<td>10.000</td>
<td>-34.3</td>
</tr>
<tr>
<td>15.000</td>
<td>-34.2</td>
</tr>
</tbody>
</table>

8.6.2 Platform measurements

While the measurements with the antenna under the platform were taken, the rig was drilling and although the rotary was not driving any load, it was turned on to maximise the man-made noise. Most of the motor controllers used silicon controlled rectifiers (SCRs), which produce significant amounts of low frequency noise when switching. The drilling in this particular case was performed by a mud motor. After switching the spectrum analyser to max-hold mode, 3 or 4 sweeps were collected so as to capture the worst-case noise.

Figure 8.11 shows a wide sweep from 9 kHz to 30 MHz.

Figure 8.11. Measured noise spectrum from 9 kHz to 30 MHz.
Figure 8.12 shows a sweep from 10 to 15 MHz.

Figure 8.13 shows a sweep around a centre frequency of 13.56 MHz.

With reference to Figure 8.13, the maximum noise was -45.95 dBm or 61.04 dBµV at 13.605 MHz yielding a magnetic field of 26.79 dBµA/m or 21.85 µA/m. This large peak in the region was most probably due to a local broadcast as the band 13.600 to 13.800 MHz is designated as “broadcasting”. Should such interference...
be considered detrimental, the lower sideband could be considered with a maximum noise of -85 dBm or 21.99 dBµV (peaks just below 13.56 MHz and just above 13.06 MHz) yielding a magnetic field of -12.26 dBµA/m or 243.8 nA/m.

### 8.7 Available source power in octagon antenna field

A larger diameter loop antenna that was better suited to the application was constructed as an octagon from eight plates of aluminium (100 mm × 250 mm × 3 mm), this octagon antenna can be seen in Figure 8.14.

The antenna had an inductance at 13.56 MHz of 976.2 nH ($r_s = 1.1484 \, \Omega$) and was matched to 50 Ω with a Q factor of 10.2. The network analyser trace shown in Figure 8.15 shows the 7 dB points of the return loss which corresponds to the 3 dB points of the tuned circuit. The two single-turn coils, one on a core with legs and one on a core without, were placed in a well itself placed in the centre of the octagon antenna with 10 W of input power as shown in Figure 8.14. The magnetic field at 10 m with 10 W of input power into this antenna with its axis vertical (as it would be in its fixed mounting location) was measured to be 18.73 dBµA/m, which was well under the allowed field (42 dBµA/m at 10 m) for this frequency (FCC 2008, ETSI 2010).
Figure 8.15. Octagon antenna return loss.

Table 8.3. Power measurements for single-turn solenoid in the deep well, $H_{\text{average}} = 3.1725$ A/m at the well edge.

<table>
<thead>
<tr>
<th>Well parallel to octagon antenna edge</th>
<th>$P_{\text{coil}}$ dBm</th>
<th>$P_{\text{corrected}}$ dBm</th>
<th>Increase dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>No legs</td>
<td>-18.67</td>
<td>-18.18</td>
<td>0</td>
</tr>
<tr>
<td>With legs</td>
<td>-2.95</td>
<td>-1.66</td>
<td>16.52</td>
</tr>
</tbody>
</table>

The results of received power, measured with the spectrum analyser, from the two single-turn coils, one on a core with legs and one on a core without, in the deep well are in Table 8.3.

The available source power of -1.66 dBm for the coil with legs in the deep well was 0.84 dB more than the -2.5 dBm required to operate the chip strongly.

The close-field probe was used in turn to measure the field at the well edge (at top of apparatus) with the coil with legs and the coil without legs in place. The magnetic field was 3.15 A/m (no legs) and 3.195 A/m (legs) which gives an average of 3.1725 A/m, when the octagon antenna is driven with 10 W.
8.8 Reduced depth of the well

Another centre section of the test well was fabricated, with the depth of the well reduced by 7.5 mm (which was the length of one of the ferrite pieces forming the legs). This is to simulate the wearing of the drill string in use. The coil with legs had 7.5 mm taken off the length of the legs by removing one piece of ferrite from each leg. The coil was brought to resonance by a shunt capacitance. The coil without legs was left unmodified and brought to resonance similarly. A photograph of the modified single-turn coil with legs, the reduced-depth well (housing the coil without legs), and the original centre piece is shown in Figure 8.16.

The network analyser traces of Figures 8.17, 8.18, 8.19, and 8.20 show the voltage reflection factors, for both inductance and dynamic impedance at resonance, of the two single-turn coils (one with legs and one without legs) in the reduced well.

The impedance of the coil without legs in the shallow well is shown in Figure 8.17, and the impedance with parallel resonance with a capacitor placed close to the back of the well is shown in Figure 8.18.

Using the dynamic impedance from Figure 8.18, the voltage reflection factor for the coil without legs was:

\[ \Gamma = \frac{Z_1 - Z_0}{Z_1 + Z_0} = 0.332 \]
This implies that 11.0 % of the power was reflected and the received-power correction factor to obtain the available source power was 1.124 (0.51 dB).

The impedance of the coil with legs in the shallow well is shown in Figure 8.19, and the impedance with parallel resonance with a capacitor placed close to the back of the well is shown in Figure 8.20.

Using the dynamic impedance from Figure 8.8, the voltage reflection factor for the coil with legs was:

\[ \Gamma = \frac{Z_l - Z_0}{Z_l + Z_0} = 0.460 \]

This implies that 21.2 % of the power was reflected and the received-power correction factor to obtain the available source power was 1.268 (1.03 dB).

The two single-turn coils (one with legs and one without legs) in the reduced-depth well were placed in the centre of the octagon antenna with 10 W of input power and the received power measured with the spectrum analyser. These measurements appear in Table 8.4. Once again the reflection factor between the test coil and the spectrum analyser was taken into account so the available source power of the coil was calculated as \( P_{\text{corrected}} \).

The available source power of -0.57 dBm for the coil with legs in the shallow well was 1.93 dB more than the -2.5 dBm required to operate the chip strongly.
Figure 8.18. Dynamic impedance of test coil without legs in shallow well.

Figure 8.19. Impedance of test coil with legs in shallow well.
Chapter 8

A Drill String Identification Tag

Figure 8.20. Dynamic impedance of test coil with legs in shallow well.

Table 8.4. Power measurements for single-turn solenoid in the shallow well, $H_{\text{average}} = 3.1725$ A/m.

<table>
<thead>
<tr>
<th>Well parallel to octagon antenna edge</th>
<th>$P_{\text{coil}}$ dBm</th>
<th>$P_{\text{corrected}}$ dBm</th>
<th>Increase dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>No legs</td>
<td>-9.96</td>
<td>-9.45</td>
<td>0</td>
</tr>
<tr>
<td>With legs</td>
<td>-1.60</td>
<td>-0.57</td>
<td>8.88</td>
</tr>
</tbody>
</table>

8.9 Empirical results

The following two sections summarise the empirical results of measurements on coils in a well; the amount of detuning of untuned coils, and the change in available source power from tuned coils excited by a magnetic field.

8.9.1 Amount of detuning

The inductance for the coil without legs changed from 22.1 nH in a deep well to 22.6 nH in a shallow (less 7.5 mm) well. Therefore the change from deep to shallow resulted in a 2.3 % increase in inductance.
The inductance for the coil with legs changed from 51.7 nH in a deep well to 41.4 nH in a shallow (less 7.5 mm) well. Therefore the change from deep to shallow resulted in a 20% reduction in inductance.

### 8.9.2 Change of available source power

The advantage in available source power by placing legs on the coil in a deep well was 16.52 dB.

The increase in available source power for the coil with legs going from a deep to a shallow well was 1.09 dB.

The advantage in available source power by placing legs on the coil in a shallow well was 8.88 dB.

The increase in available source power for the coil without legs going from a deep to a shallow well was 8.73 dB.

### 8.10 Design of a tag

Since the coils with legs achieved available source powers above that required for strong chip operation, a tag using coils with legs was designed to start in a deep well and, after drill string wearing, end in a shallow well. The tuning capacitor would be fixed so the coil in the deep well would start with a low resonance frequency and the coil in the shallow well would end with a high resonant frequency. Providing the chip voltage was adequate for correct chip operation for both the low and high resonant frequency cases, the result would be a workable tag solution.

Using the measured impedance data for the single-turn coils with legs in the deep (see Figures 8.7 and 8.8) and shallow wells (see Figures 8.19 and 8.20), the tag equivalent circuits were simulated in SPICE. The chip requires 2.1 V\text{peak} across an input impedance of 3.5 k\Omega for strong subcarrier operation.

Both coils with legs were initially resonated to 13.56 MHz by the addition of a shunt capacitance, and the chip load represented by the addition of a shunt resistance of 3.5 k\Omega. The coil with legs in the shallow well had an available source power of -0.57 dBm (see Table 8.4) which is 1.93 dB above the chip’s strong operating point of -2.5 dBm, so the induced coil voltage was adjusted to achieve 2.62 V\text{peak}. The coil with legs in the deep well had an available source power of
-1.66 dBm (see Table 8.3) which is 0.84 dB above the chip’s strong operating point, so the induced coil voltage was separately adjusted to achieve 2.31 V\text{peak}, since this coil had a different inductance and a different coupling to the inductance of the field creation loop. These coil calibrations from the measured results can be seen in Figure 8.21.

A fixed resonating capacitance for both coils was chosen to give the same chip input voltage for both coils at 13.56 MHz. The resonant frequencies had now shifted, below the carrier for the deep well and above the carrier for the shallow well. This resulted in reduced chip voltage at 13.56 MHz for the single-turn coils as can be seen in Figure 8.22.

To form 4-turn coils \((N = 4)\) the resonant circuit parameters for both deep and shallow coils were scaled as follows:

- the 1-turn coil’s inductance was multiplied by 16 \((\times N^2 \text{ for more turns})\)
- the 1-turn coil’s series resistance was multiplied by 4 \((\times N \text{ for more turns})\)
- the shared fixed capacitor for the 1-turn coils was divided by 16 \((\times 1/N^2 \text{ to maintain resonant frequency})\)
- the individual induced coil voltages of the 1-turn coils were multiplied by 4 \((\times N \text{ since the induced voltage is } j\omega MI, \text{ where } I \text{ is the current in the excitation inductor, and the mutual inductance } M \text{ between the excitation inductor and the tag coil is } \propto \sqrt{L_{\text{excitation}}L_{\text{tag}}})\)

The resulting tuning for each 4-turn coil is shown in Figure 8.23.

### 8.11 Construction of a tag

Although a 4-turn coil from simulations looked to be sufficient, extra margin was desired for the tag so a 5-turn coil was chosen for fabrication. A tuned circuit with a Q factor of approximately 30 and a dynamic impedance of around 3.5 k\(\Omega\) was desired. This would achieve maximum power transfer to the ISD 6408 hybrid whose input impedance is around 3.5 k\(\Omega\). A Q of 30 was chosen to yield a working Q of 15 which gives a \(\Delta f\) of 900 kHz.

A 5-turn coil of 0.8 mm diameter enamelled copper wire was wound on a ferrite core “with legs”, with a tuning capacitor and hybrid behind the bottom of the test
Figure 8.21. Simulation calibration from measurements of 1-turn coils.
Figure 8.22. Addition of fixed capacitance to 1-turn coils.
Figure 8.23. Simulation of 4-turn coils.
well, inside the apparatus so as to not perturb the field. A short length of coax joined the coil to the bulkhead connector so the inductance could be measured with the network analyser. The inductance of the tag coil inside the deep well at 13.56 MHz was 1.2721 \( \mu \)H, with a series resistance of \( r_s = 3.7344 \) \( \Omega \).

The shallow well was chosen first since the coil in this well would have the most coupling to the field creation antenna. The drill string model fitted with the shallow well and the matching tag coil with the shorter legs was placed in the centre of the octagon antenna which was connected to an ISD Model 5000 reader operating at 8 W.

The baseband signal was monitored with the Tektronix TDS 544A digitising oscilloscope to record the frequency of the ISD 6408 chip’s voltage dependent oscillator which when at a frequency of 200 kHz is considered to give a strong tag reply. A resonating capacitance added at the back of the shallow well was adjusted to give the tag both a resonant frequency higher than the 13.56 MHz carrier, and a voltage dependent oscillator frequency of 200 kHz.

The drill string model was then switched to contain the deep well and the matching tag coil with the longer legs. The same shunt capacitor which was adjusted for the shallow well was connected to the coil at the back of the deep well. The voltage dependent oscillator of the ISD 6408 chip was running at 232 kHz, higher than the 200 kHz which is considered to give a strong reply.

The tag tuning was thus skewed to favour the deep well, where the coupling to the field creation antenna would be less than that for the shallow well.

### 8.12 Numerical analysis of a tag in a metal well

The same ferrite material as used in the empirical experiment described originally in Section 8.2 but restated in Table 8.5 along with the other parameters were used to model the metal well in HFSS simulations.
Figure 8.24. Model of the ferrite coil.

Figure 8.24 shows the U-shaped ferrite core with a single 6 mm width turn, the red and blue regions at the gap represent the feed point and shunt tuning capacitance.

Figure 8.25 shows the ferrite coil inside the hole, which is modelled by placing conductive boundaries with the properties of brass, at the appropriate 5 sides of the well. The boundaries have no drawn thickness, the simulator assumes they are semi-infinite in thickness.

Figure 8.25. Model of the ferrite coil in a brass well.
Figure 8.26. Model of the ferrite coil in a brass well with the well entry represented as a radiation surface.

Figure 8.26 shows a radiation surface across the well entry. Fields exiting the well via the radiation surface are allowed to radiate freely in the external hemisphere. In this way the meshes are able to be small within the well of 25.5 mm maximum dimensions, without requiring a large simulation volume of some 3.5 m radius at 13.56 MHz outside the model to allow the magnetic near fields to form before they are interrupted by a boundary surrounding the whole simulation volume.

Results for the simulation of the coil with legs, as shown in Table 8.6, predict around 0.5 dB less increase in available source power than the empirical measurement stated in Section 8.9.2 and also given in Table 8.6, which suggests the modelling can assist in the design of a more-snug-fit ferrite core.

<table>
<thead>
<tr>
<th>Depth</th>
<th>Ferrite without legs</th>
<th>Ferrite with legs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Raw Prad mW</td>
<td>5.766</td>
<td>36.767</td>
</tr>
<tr>
<td>Accepted P mW</td>
<td>582.610</td>
<td>547.850</td>
</tr>
<tr>
<td>Corrected Prad mW</td>
<td>9.897</td>
<td>67.111</td>
</tr>
<tr>
<td>Modelled increase dB</td>
<td>0</td>
<td>8.31</td>
</tr>
<tr>
<td>Empirical increase dB</td>
<td>0</td>
<td>8.73</td>
</tr>
<tr>
<td>Waveguide increase dB</td>
<td>0</td>
<td>8.06</td>
</tr>
</tbody>
</table>
The simulator was used to model the effect of wear in the well depth on a fixed tuned tag. For a shunt capacitance of 870 pF on the single-turn coil with legs, the tuning was arranged for a resonance above 13.56 MHz in the starting depth well, and as the well wears the reflection coefficient passes through resonance to a tuning point more below the carrier but as the well depth reduces attenuation also reduces, so the same radiation from the well is produced at its starting depth and its fully worn depth. These tuning points in a 50 Ω system are shown in Figure 8.27.

Figure 8.27. Start (+) and Finish (□) tuning points of the coil with legs which after well depth wear resulted in the same tag coupling.
8.13 Summary

The difference in available source power, of a ferrite coil without legs at the bottom of the well, between a deep and a shallow well was measured at 8.73 dB, as stated in Section 8.9.2. The difference of 8.06 dB from Equation 8.1 of Section 8.2 for a lossless well is a good prediction of the expected loss.

The increase in available source power for the coil with legs starting in a deep well and ending in a shallow well was 1.09 dB measured and 0.55 dB simulated. These small increases as the well changes its depth due to wear in use meant the coil with legs was suitable for a tag.

A successful design was validated in a real drill string environment. Detuning and coupling changes as wear occurs have been modelled.
The current reference is a key building block of low-power analogue microcircuits. This chapter describes the circuitry developed by the author for a self-starting stable current reference. The circuit has been widely used in fabricated chips.
9.1 Introduction

Further to prior published work (Hall and Cole 1997) a low-power current reference was developed that was not only stable when large parasitic capacitance from the use of on-chip well resistors is present, but was self-starting in a short time so as to be usable in a passive (Razban et al. 1987, Turner 1993) RFID chip.

9.2 MOSFET operation in weak inversion

The resistor R1 in Figure 9.1 sets the current through P1 and P2 according to the relation:

\[ I_{R1} = \frac{V_T}{R1} \ln \frac{K}{R1} \]

where \( K = \left( \frac{W}{L} \right)_{N2} \left( \frac{W}{L} \right)_{N1} \)

\( V_T = \) thermal voltage \( = kT/q \approx 26 \text{ mV at } T = 300 \text{ K} \)
\( k = \) Boltzmann constant \( = 1.38066 \times 10^{-23} \text{ J/K} \)
\( q = \) the magnitude of the electron charge \( = 1.6021765 \times 10^{-19} \text{ C} \)

In the above relation the current is independent of the supply and in practice provides relatively constant current for changes of \( V_{DD} \). The capacitor C1 in Figure 9.1 represents the parasitic capacitance at that node due to: the PN junction capacitance of a well resistor; the track to substrate capacitance of an interconnecting metal layer track; the pad capacitance and/or package pin capacitance which may exist for external resistor connection; or any connected measuring device.

The gate voltages of Vbp of P1 and Vbn of N1 are used to bias the gates of P-type and N-type MOSFETs to mirror the reference current for current sources and sinks respectively. These mirrored slave transistors may have their current values adjusted by the ratio of their \( W/L \) with respect to the \( W/L \) of P1 for a source or N1 for a sink.

9.3 Circuit stability

Due to positive feedback in the operation of this current source, care must be taken during measurements of sensitive nodes. The node connecting R1 to the source of N2 is such a sensitive node, and added capacitance to ground can cause the current source to oscillate. A simple analysis neglecting all parasitic capacitances gives the impression of positive feedback with a DC loop gain less than unity, therefore stability is assumed.
An analysis identifying parasitic capacitances generally concludes that the net effect of transistor capacitances give phase lag as well as contributing to a reduction in gain. Should significant capacitance be present as $C_1$, a net phase lead and an AC gain greater than unity can occur leading to oscillations. In simulation, node A of Figure 9.1 is broken and an input 1 mV peak AC test signal is applied to the gate of N2, with the output taken from the drain-gate node of N1. Figures 9.2 and 9.3 show the magnitude of loop gain in $V/V$ (top trace), and phase response in degrees (bottom trace) against frequency $f$ in Hz.

Figure 9.2 can be seen to have a loop gain greater than unity with some low frequency phase lead. For Figure 9.2, 25 pF has been added as $C_1$ with an $R_1$ of 1.5 MΩ and a $V_{DD}$ of 3 V. At face value this capacitance seems high but is of the order of parasitic capacitances of CMOS well resistors.

When significant capacitance $C_1$ exists, addition of sufficient capacitance between $V_{DD}$ and the gate of P2 puts back the phase lag and reduces loop gain as seen in Figure 9.3. For Figure 9.3, 15 pF is placed in this position. This capacitance may be implemented by an explicit added capacitor, or by increasing the geometry of transistor P2. The most economical method in terms of area is dependent on whether a digital process or an analogue process (where high-value capacitors may be formed in a reasonable area) is used for the fabrication of the circuit.
The current reference shown in Figure 9.1 should self-start as long as the leakage of transistor N2 is greater than that of N1. This can be ensured by increasing both the width and length of N2. There is some discrepancy in published views as to whether the state which has zero current through both branches is a stable (Allen and Holberg 1987) operating point or an unstable (Vittoz et al. 1985) operating point. Empirical observation by the author suggests that with appropriate transistor sizes this zero-current state is an unstable operating point and that the circuit will reach a desired equilibrium some time after power has been applied. Where this current reference is used as part of a battery-powered circuit (Oguey and Gerber 1980, Nicollini and Senderowcz 1991), the time to reach a stable operating point is not an issue but as a passive RFID chip is expected to operate effectively immediately upon entry to an excitation field a start-up circuit is necessary.

### 9.4 Start-up circuit

Figure 9.4 shows the addition of two N-type transistors N3 and N4, and a small capacitor Cs which ensures that upon power-up the circuit does not stay at the
zero-current operating point. As the supply voltage increases from a zero value, capacitor Csu pulls the node cstart high, turning on start-up transistor N4, causing current to flow through transistor P1 and the diode-connected transistor N1, whose gate voltage vn causes current to flow through transistor N2 and transistor P2, thus starting the current reference. The voltage vn turns on a discharge transistor N3 which pulls cstart low turning off start-up transistor N4. The additional start-up transistor N4 and discharge transistor N3 only conduct during start-up, when the supply voltage initially increases, and do not affect the operation of the current reference once it has started and the supply voltage has settled to its operating value. The capacitor Clag ensures that the circuit is stable with the parasitic capacitances of the resistors Rnwell and Rpoly which capacitances add to the total capacitance between the node res and Vss.

The nominal 64 kΩ resistor is made from a wire of polysilicon and a wire of Nwell, the two resistors have different temperature coefficients and by being in this split form the current in mirrored slave stages used in the biasing of other circuits remains quite constant over temperature and voltage variations. The N-well resistor is slightly voltage dependent as it effectively gets thinner as the voltage across
it rises, so for this reason it has one end connected to the ground supply rail. This also helps in directing stray substrate carriers into the ground supply with only a small effect in the voltage drop across this resistor and hence the current of the reference.

The current reference used in an EM Marin 0.5 µm process is shown in part in Figure 9.5. The node \( v_p \) is the bias voltage for current sources, the node \( v_n \) is the bias voltage for current sinks, and a 250 nA sink is shown. The bias voltage \( v_n \) is not taken directly from the reference, but rather from a slave stage biased by \( v_p \). This was done since the node at the gates of the N-type MOSFETs of the reference is sensitive to noise.

The split resistor used in circuits fabricated in an EM Marin 0.5 µm process is shown in Figure 9.6, and is connected to the node \( res \).
Figure 9.5. Current reference with slaves (EM Marin 0.5 µm).
9.5 Summary

The basic current reference was improved by adding capacitance to prevent the circuit from oscillating when the resistor has large parasitic capacitance. A split resistor using polysilicon and well-diffusion allows the current to remain constant over temperature, the large capacitance of the well-diffusion requiring the aforementioned added capacitance to prevent oscillation. A start-up circuit was developed so that passive RFID circuits could power-up quickly as they enter a field or as a field is pulsed on.

The circuit has been successfully fabricated and used in the following chips, the analogue circuits of which were developed by the author.

- ISD AC128 - battery assisted UHF chip - Orbit 2 μm.
- ISD 72128 - passive HF chip - Chartered Semiconductor 0.8 μm.
- TAGSYS C220 - passive HF chip - Chartered Semiconductor 0.8 μm.
- TAGSYS C310 - passive HF chip - EM Marin 0.5 μm.
- TAGSYS C320 - passive HF chip - EM Marin 0.5 μm.
Chapter 10

Random-Number Oscillator

Tags which use an ALOHA reply scheme, where tag replies are offered on a periodic basis with a low duty cycle so as to allow time for other replies to occur without collision, require some kind of oscillator to allow and disallow replies. In HF slotted ALOHA reply schemes timing is derived from the energising carrier and non-overlapping slots can be allocated by dividing down the carrier, and can be synchronised by a pulsed field or a command issued from the reader. For this latter case some method is required to select a reply slot from a number of slots on a random basis so that over time a group of tags may choose different slots so their replies may be detected by the reader without collision. This chapter describes the design of two elements required for a random-number generator for an HF system, an unstable oscillator and a stable signal source of higher frequency.
10.1 Introduction

Tags using an ALOHA anti-collision method for their time to reply require some method by which to select a time. Early designs simply used a field-dependent delay between subsequent replies which delay was derived from a reply-rate oscillator (RRO) which was really a monostable multivibrator circuit which was triggered at the end of a reply with the next reply occurring after some time had elapsed. The timing was made field-dependent by allowing either the charge current of a capacitor or the capacitor-voltage trigger threshold to vary with the supply voltage. A variation on this theme includes a voltage-dependant capacitor. The system would work by each tag having a different reply rate and not unlike watching the turn indicators of more than one automobile at a set of traffic lights the replies would sometimes overlap and sometimes interleave. By using an inter-reply time of 10 times or more the duration of a reply, practical systems could reliably detect 9 tags bunched together provided they were in the energising field for $\approx 150$ ms.

As ALOHA systems evolved a more structured approach was formed which eliminated the partial overlapping of replies that would occur in the above anti-collision approach and result in a collision just the same as simultaneously replying tags. The slotted ALOHA system contains tag reply times that are under reader control. Using this method the reader would announce the start of a slot and the slot may contain no tags, one tag, or more than one tag. After a decision had been made as to the contents of the slot, the reader would then signal the start of the next slot either immediately (no reply) or after any reply had finished. In this way time was saved by eliminating empty slots but more importantly, tags that would have their replies collide would do so completely, eliminating the numerous partial overlap cases of collision from the older ALOHA method.

Thus for a slotted ALOHA anti-collision system to operate a method for randomly selecting a slot out of some total number was required. The approach taken at 13.56 MHz was to sample the well-controlled carrier frequency, or in this case the divided-by-2 6.78 MHz, with a slower not-so-well-controlled oscillator or unstable oscillator. The divide-by-2 clock was used to assist in a more uniform 50 % duty cycle, since the analog 13.56 MHz input was required to be interfaced to the on-chip voltage which can introduce an asymmetry in the duty cycle, along with the condition that the on-chip ground and supply nodes float about with respect to

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7 A library solution utilising the TAGSYS C220 chip.
Chapter 10

Random-Number Oscillator

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Figure 10.1. Random number from a noise source.

the only input terminals, the connections to the antenna, with the action of a full-wave rectifier. The near 50% duty cycle eliminates the need for extra averaging circuitry.

The theory (Fairfield et al. 1984) of random number generation using this method relates the standard deviation of the unstable oscillator’s period to the period of the stable reference.

If the standard deviation of the unstable period is greater than that of the reference period, the circuit has an approximately even chance in choosing a 1 or a 0 for each consecutive bit. This means the choice of a bit approaches that of a true random choice and is not dependent on the previous choice. Figure 10.1 shows the concept from Intel’s (Jun and Kocher 1999) random-number generator.

Figure 10.2 shows a technique for generating random numbers in hardware, where a long period clock modulated by random noise is used to stop the count of a short period clock. Variation due to noise of the timing of consecutive triggering edges of the long period clock results in different numbers of the short periods. It is this method that was used to generate the random data by sampling a stable 6.78 MHz clock with an unstable oscillator. The shortest “long period”, the shortest count, must include more short periods than the decimal quantity of the maximum random number. For example, in the TAGSYS C310 chip for which the analogue circuits were designed by the author, the number of ALOHA slots is 16, therefore during the shortest counting event it is desirable to have the number of short periods N greater than 16 so that the count ends up being N modulo 16. This way even a short count-clock period may result in a large random number.
10.2 Designing an unstable oscillator

When the author designed the analogue circuits of the TAGSYS C220 chip, much work was done in creating a stable asynchronous oscillator with respect to on-chip voltage and temperature variations which affected the current used to charge a capacitor of an integrator-type oscillator. This chip also included an integrator-type monostable for chip reply timing which was desired to vary with on-chip voltage so that the replies from a group of tags would be separated in time to achieve a simple anti-collision scheme.

As an HF chip moves through a field the induced coil voltage possibly goes through some 44.7 dB of dynamic range while the chip operates. The on-chip regulator strives to keep the voltage below device breakdown, so inevitably there is some variation in on-chip voltage. This variation in on-chip voltage is exploited to create variations in the periods of a free-running oscillator.

The first approach in the unstable oscillator design was to avoid any voltage compensation and promote changes with temperature in the mirrored current from an otherwise temperature compensated reference (the main current reference was used for other circuits and was therefore made quite stable), eliminating the need for a separate area hungry current reference.
The oscillator was laid out without the usual guard rings to promote temperature dependent leakage currents to nodes other than the supply rails, with short transistors in the current mirrors (to promote current variation with voltage). The circuit was also powered from an on-chip analogue supply derived from the RF which varied between 2.5 to 7 V with varying energising field, again to promote some variation in oscillator period. Long transistors, formed using a serpentine structure to conserve space and form cells of similar height for easy interconnect and power rail connection, were laid out vertically with current flow in the direction perpendicular to the well-substrate boundary. Using diffusion to connect between segments rather than using metal causes significant error in the current match due to leakage at low transistor currents, with the error increasing with temperature and voltage. Although undesirable normally, it is desired in the unstable oscillator design to promote a spread in oscillator periods.

Alas the early prototypes failed to meet the requirement of a large standard deviation; it proved difficult to make a poor oscillator.

Later successful designs, described further below, led to the definition of the following methods for increasing the voltage variations on an oscillator, which methods were used in those designs.

1. For current mirror slaves, use the thinnest transistors of the process and use the longest length transistors that have been characterised in manufacturer data or SPICE files. Don’t mirror with the same geometry as the current reference source.

2. Use as many transistors in series as the minimum supply voltage allows (this includes AM modulation dips).

3. For transistor switches and pass transistors use minimum geometry transistors.

4. Reduce the number of well and substrate connections to the supply rails, a successful technique is to surround the design “wells” with a fence of the appropriate diffusion with a few connections along the supply rails, leaving the internal area free from connections. This way the guard rings help to protect the circuit from stray carriers but allow devices to be a long way from a substrate connection.
5. Organise series transistor strings to be “tall” and orthogonal to the supply rails so that the transistor at the “end” of the series stack is a long way from a substrate connection.

6. Place single connections to one side of a wide transistor’s drain and source so there are parallel stronger and weaker pathways through the transistor.

7. For logic gates, use the gate which uses as the series transistors those which have the largest variation in conduction with voltage.

10.3 Clock extraction from the carrier

Figure 10.3 shows a pseudo NMOS inverter used for the conversion of the AC voltage at the antenna terminals to a squarewave (with some edge slew) of the same frequency at the supply voltage. The squarewave is then applied to a divide-by-2 circuit (see Figure 10.4).

A simple inverter was not suitable for the AC voltage conversion because during reply modulation the peaks of the AC antenna voltage dropped close to the inverter switching point. Also, a simple inverter clock extractor required small
Figure 10.4. Branch-based logic divide-by-2 circuit.
transistor sizes for low current operation but required large transistor sizes to
drive the input capacitances of the circuits connected to the output. This resulted
in mutually exclusive design targets.

Consideration of a two-inverter stage carrier extractor was given but the added
area was a negative along with only a slight current consumption advantage (over
the pseudo NMOS) at a higher supply voltage than that necessary in order to not
miss a carrier cycle during modulation.

A pseudo NMOS design conceptually has a high current draw, but at high fre-
quencies its current draw is acceptable. The pseudo NMOS inverter allows a large
capacitance to be driven at high frequency with an input voltage swing between
zero and not much more than an N-type threshold voltage, and all at a lower
supply voltage.

Figure 10.4 shows a dedicated divide-by-2 circuit based on branch-based (Piguet
1995) logic. This form of logic is a state driven logic with gates that when an in-
put changes an output, feedback reinforces the input change causing that output,
similar to a master-slave operation. This means that there are no fight conditions
where a pull-up and pull-down occur simultaneously when an input is halfway
between the supply rails. This avoidance results in low current consumption.

In order to assess the current consumption of the dedicated divider, a comparison
was made against the branch-based divider and a standard cell D-type flip-flop
provided by the foundry. The circuits were simulated at a $V_{DD}$ of 1.45 V with a
worst-case 13.56 MHz sinewave input with a $V_{DD}/2$ peak and a $V_{DD}/2$ DC offset.
The result was a 0.605 $\mu$A consumption for the branch-based design, and 1.099 $\mu$A
for the standard D-type flip-flop cell.

10.4 An unstable oscillator

An unstable oscillator circuit was prototyped and constructed on EM Marin’s
0.5 $\mu$m digital process. Two integrator-type asynchronous oscillators of slightly
different nominal frequencies (by using different values of timing capacitor) with
equally poor layout techniques had their outputs mixed together as described be-
low to form a single clock with FM-like variations in frequency. This unstable
oscillator was then used to sample the count of a stable 6.78 MHz clock, derived
by dividing down from the received carrier of frequency 13.56 MHz +/- 50 ppm.

Digital mixing is often performed with an XOR gate, and as can be seen in Fig-
ure 10.5, typical implementations of XOR gates involve many transistors.
A NOR gate (see Figure 10.6), which uses fewer transistors than an XOR gate, was tested as a mixer in a SPICE simulation, and the result was compared against that of an XOR gate (see Table 10.1).
### Table 10.1. Comparison of XOR and NOR gates for asynchronous oscillator mixing.

<table>
<thead>
<tr>
<th>NOR</th>
<th>XOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unstable period $T \mu s$</td>
<td>6.78 MHz periods</td>
</tr>
<tr>
<td>9.765</td>
<td>66.2</td>
</tr>
<tr>
<td>3.487</td>
<td>89.8</td>
</tr>
<tr>
<td>6.031</td>
<td>130.7</td>
</tr>
<tr>
<td>6.027</td>
<td>171.6</td>
</tr>
<tr>
<td>7.694</td>
<td>223.6</td>
</tr>
<tr>
<td>7.750</td>
<td>276.3</td>
</tr>
<tr>
<td>2.577</td>
<td>293.8</td>
</tr>
<tr>
<td>6.034</td>
<td>334.7</td>
</tr>
<tr>
<td>6.875</td>
<td>381.3</td>
</tr>
<tr>
<td>7.785</td>
<td>434.1</td>
</tr>
<tr>
<td>3.267</td>
<td>456.2</td>
</tr>
<tr>
<td>6.036</td>
<td>497.2</td>
</tr>
<tr>
<td>6.175</td>
<td>539.0</td>
</tr>
<tr>
<td>7.758</td>
<td>591.6</td>
</tr>
<tr>
<td>4.027</td>
<td>618.9</td>
</tr>
</tbody>
</table>

- **Average unstable period** $T_{ave} \mu s$: 6.086
- **Unstable standard deviation** $\sigma \mu s$: 2.008
- **Stable clock period** $T_{6.78MHz} \mu s$: 0.147

- **Average unstable period** $T_{ave} \mu s$: 6.804
- **Unstable standard deviation** $\sigma \mu s$: 1.951
- **Stable clock period** $T_{6.78MHz} \mu s$: 0.147
Since the results (see Table 10.1) for mixing revealed that the XOR gate, which has equal numbers of high and low logic outputs in its truth table, offered no real improvement in oscillator period variation and required a larger area and increased current consumption a NOR gate was chosen.

It can be seen from the last rows of Table 10.1 that the standard deviation of consecutive unstable oscillator periods is greater than the period of the stable clock. This result means that each bit was chosen at random and was not determined by the previous choice.

The NOR gate has the benefit in this application of the weaker P-type transistors being in series, so the switching delay should be more voltage dependent than the alternative NAND gate. Although repeat simulations of a circuit netlist with unchanged input parameters gives the same result each time, simulations are useful in order to create the basic circuit. Real validation is performed empirically after fabrication.

The circuit of Figure 10.7 shows an unstable oscillator with a shared reference. In an attempt to cut down on the number of current mirrors contained in the circuit, pass transistors were used to connect the comparators to upper and lower voltages from a common reference. Along with the current and area saving, this was trialled to see if each oscillator would effect the other’s reference voltage and therefore switching point for “extra” uncertainty of the periods. At large supply voltages (around 5 V), capacitive coupling from the pass transistors back to the common reference meant that the faster of the two oscillators would vary the common reference with the result that the slower oscillator would speed up and become synchronised to the (initially) faster oscillator.

It turned out that the interaction resulted in the two oscillators “settling” to relatively constant frequencies. At moderate to high excitations, each time a timing capacitor voltage reached the “high” reference and switched to discharge towards the “low” reference the other capacitor was forced to change charging direction.

The results for a choice of 1 in 16 slots shown in Figure 10.8 shows a poor result. The results were taken by a TAGSYS L200 reader while power into a 300 mm square loop was slowly cycled through 28 steps from 250 mW to 7 W reader power. This represents around 14.5 dB variation for a tag in a fixed position.
Figure 10.7. Unstable oscillator with shared reference.
Figure 10.8. Results for unstable oscillator with shared reference.
10.5 An improved unstable oscillator

In order to make the distribution of chosen slots more uniform, two changes to the unstable oscillator were proposed. A second reference was added such that the outputs of two totally independent oscillators were mixed together, and the circuit was run from a digital supply which varied between 2 to 4 V (with excitation field), giving redundancy in the protection against synchronisation.

The circuit of Figure 10.9 shows an unstable oscillator with individual references for the integrator oscillators. Here each free-running oscillator is as independent as possible, and the only intentional interaction is a final mixing of the two oscillators.

Figure 10.10 shows the much improved results. The slots chosen by the tag are not too far from a uniform distribution which is suitable for the 1 in 16 slot number generator.

10.5.1 Long-term asynchronous oscillator stability

There are two stabilities to consider, instantaneous or more correctly short-term stability and long-term stability. The long-term stability is not particularly relevant to an RFID system, as the tag is usually not in the field for long periods of time, but was measured to see if any undesirable oscillator behaviour occurred after a tag was powered for a “long time”. Even in an anti-collision system with 1024 slots if the tag took 10 rounds to reply in a clear slot, the tag active time would be $\approx 200 \text{ ms}$.

Figure 10.11 shows the long-term stability of the unstable oscillator with individual references, powered at RF at maximum range.

The unstable oscillator periods were collected for 300 $\mu$s every 30 seconds for 10 minutes, and one further data point was taken after 20 minutes. The circuit’s standard deviation of about 600 ns remained greater than the 6.78 MHz clock’s period of 147.5 ns for up to 20 minutes, which means the choice of each bit is random and not determined by the previous choice.
Figure 10.9. Unstable oscillator with separate references.
Figure 10.10. Results for unstable oscillator with separate references.
Figure 10.11. Long-term stability of the asynchronous low frequency oscillator (separate references).
10.6 Summary

Two circuit elements of a random-number generator were designed: a stable signal source using an unconventional state-driven divider design with low switching current for division of a 13.56 MHz carrier; and an unstable oscillator used to sample the stable signal source in order to derive a random binary number. Both these circuits were successfully fabricated on an EM Marin 0.5 $\mu$m process and used in the TAGSYS C310 and C320 HF chips.
This chapter examines design variations of full-wave rectifiers for HF chips. The undesirable features of three-terminal coil and chip connections are discussed and options for two-terminal designs explored. Both the advantageous and disadvantageous features of the latter are identified. Electrostatic protection issues are also considered. A number of successful rectifier designs are described.
Chapter 11 HF Rectifiers

11.1 Introduction

The choice of rectifier architecture for an RFID chip is dependent upon the processing layers which are available to the designer. “Floating” Schottky diodes are the most efficient, and with them classical rectifier designs may be implemented. The low reverse breakdown of these diodes however requires care in regulator design. Schottky diodes in the substrate form less-efficient rectifiers, with classical three-terminal coil full-wave, and half-wave rectifier designs possible. However three-terminal coils and chip connections are undesirable due to added manufacturing costs and chip area.

The substrate diodes of a standard CMOS process are themselves less efficient but full-wave rectifiers can be designed requiring only two coil terminals. Three variations of this type of full-wave rectifier are discussed with their various advantageous features and pitfalls identified.

The design of the half-wave rectifier involving the substrate diode is trivial with only a “well” guard ring required to collect carriers injected into the substrate. Due to its inferior performance it is not discussed further.

11.2 Points to consider for rectifier design

In electronic tag standards such as ISO18000, specifically Part 3 for HF tags, a maximum operating field for a tag is 5 A/m and the tag must also be able to survive 12 A/m with a loop the size of a credit card. In the case where the chip supply voltage regulation, or limiting, is performed behind the rectifier, as in this work, there are some points to consider.

Some applications may use loop antennas larger than a credit card so the size of the largest loop antenna that will be used with a chip should be used in the calculation of the maximum RF input the chip will encounter. The operating voltage of the main circuitry which is behind the rectifier must be kept below maximum limits. A resistive load applied to the chip supply will draw current through the rectifier and the peak RF voltage at the chip’s input terminals will be higher than the chip’s supply voltage, therefore the impedance of the rectifier must be considered so as to not exceed the maximum allowed voltage at the chip input. This normally involves quite wide transistors for the rectifier to minimise the voltage drop across the rectifier during periods of high RF input.

The peak RF at the chip input may not be limited by the transistors themselves but by the oxide of on-chip tuning capacitors. As silicon technologies become
smaller in feature size, the oxide thickness between conductive layers becomes thinner. Thereby on-chip RF capacitors created by a stack of two conductive layers separated by oxide have their maximum operating voltage (Duan and Yuan 2000, Gong et al. 2002, Cheung 2001) reduced as the process feature sizes become smaller.

For an N-well process, the conduction characteristics of the vertical PNP when using P-type MOSFETs and of the lateral NPN (Zhang et al. 2000) when using only N-type MOSFETs must be considered to prevent too much carrier injection into the substrate when the chip regulation is in extreme clamping.

### 11.3 The P-switch N-diode rectifier

#### 11.3.1 The basic rectifier configuration

Figure 11.1 shows the symbolic circuit for the switched rectifier for an N-well process. Coil connections are to nodes la and lb, SW1 and SW2 represent P-type switch transistors, and D1 and D2 represent N-type diode-connected transistors. The polarity is dependent on the type of substrate and well in a single-well process, the design covered here is for an N-well process (the P-well version works equally well with all devices swapped, assuming N-type and P-type devices are equivalent between an N-well and P-well process. The opposite configuration (using N-type switches and P-type diodes) from Figure 11.1 when used in an N-well process is operable but because a diode-connected MOSFET cannot hold the BE junction voltage of the well-to-substrate vertical transistor as low as a MOSFET switch, the voltage which causes the parasitic devices to become forward biased (latchup (Kang and Leblebici 1998)) is lower. Even the configuration of Figure 11.1 needs careful treatment of the parasitics when used in conjunction with voltage limiting behind the rectifier and as the parasitic devices are highly process and batch dependent it is, generally, not a good practice to use the opposite design. There is intellectual property (Katzenstein 1988, Everett et al. 1996, Brooks 1991) on RF limiting before the rectifiers and while this allows the use of smaller rectifiers to meet the requirements of the tag circuitry, the larger size of the rectifier used herein is not too much of a burden in avoiding that intellectual property and allows simple AM detection, by monitoring dips of the chip supply voltage, to be employed. The chip’s reservoir capacitor and the chip’s load current form a built-in AM peak detector.
The basic rectifier circuit operates as follows. When $V_{la} < V_{lb}$ (Figure 11.1a) the node lb is connected to $V_{DD}$ via closed switch SW2, with the voltage at the $V_{SS}$ terminal following the voltage at la through diode D1, clamping at a forward-biased-diode voltage drop above $V_{la}$. When $V_{la} > V_{lb}$ (Figure 11.1b) the node la is connected to $V_{DD}$ via closed switch SW1, with the voltage at the $V_{SS}$ terminal following the voltage at lb through diode D2, clamping at a forward-biased-diode voltage drop above $V_{lb}$.

### 11.3.2 The CMOS realisation

Figure 11.2 shows the CMOS (N-well) realisation, and as PN junctions are not always reverse biased the major parasitics Q1, Q3, D2, and D4 are illustrated in Figure 11.3. The parasitics shown are due to the MOSFETs themselves, other layout associated parasitics will be discussed in Section 11.3.5 on guard rings.
Figure 11.2. Circuit diagram of a P-switch N-diode rectifier.

Figure 11.3. Circuit diagram of a P-switch N-diode rectifier including major parasitics.
11.3.3 Circuit operation

With reference to Figure 11.3, when $V_{la} < V_{lb}$ the gate-to-drain voltage of M3 is negative forming an inverted region in the N-well under the gate of transistor M3 connecting lb to $V_{DD}$ with an increasing conductance as $V_{la}$ becomes more negative with respect to $V_{lb}$. The voltage at the $V_{SS}$ terminal follows the voltage at la through both the drain-to-substrate diode D2 and the diode-connected MOSFET M2. Depending on the particulars of the process and size and layout of the MOSFET, either the drain-to-substrate diode or the MOSFET channel may conduct first and either may dominate conduction at full swing of the input voltage. It will be shown later in the all N-type rectifiers that benefits are gained by ensuring that the MOSFET has higher conductance than the drain-to-substrate diode. As the voltage at lb continues to increase with respect to that of la and $V_{SS}$, a voltage drop occurs across the drain-to-source of M3. Should this voltage cause the BE junction of the vertical parasitic Q3 to become forward biased, current will flow directly from lb (emitter of Q3) to $V_{SS}$ (collector of Q3) clamping the input RF. The RF voltage at which this occurs is a function of the clamped value of $V_{DD}$, the gain (width) of the P-type MOSFETs and the gain of the vertical PNP bipolar. Keeping the drain-to-source voltage of M3 low enough to prevent the drain-to-well (emitter-to-base of Q3) junction through its associated series resistances from being continually forward biased is the main factor dictating this MOSFET’s width. Short periods of conduction through Q3 until the MOSFET M3 takes the main current are expected and acceptable.

This rectifier has been successfully fabricated in 3 $\mu$m Hughes P-well, 2 $\mu$m Orbit P-well, 1.5 $\mu$m American Microsystems Inc. N-well, 0.8 $\mu$m Hewlett Packard N-well, and 0.8 $\mu$m Chartered Semiconductor N-well technologies. When tried in a 0.5 $\mu$m technology more care in the N-well treatment and P-type layout was required as the reduced N-well depth caused the parasitic vertical PNP to have a greater gain than the parent P-type MOSFET when a typical linear (drain gate source) layout was used. This effect is not specific to a process but is caused by reduced N-well depth due to a general shrinkage of features for a smaller feature size process.

Circular MOSFET layout increases the channel to parasitic-emitter area ratio. Semi-circular layout is required if contacts to the gate cannot be placed over the gate oxide. Due to the restriction of the over-voltage protection being on the DC side of the rectifier, a current capability of 10 mA (a value empirically derived from a maximum magnetic field of 12 A/m and a 6-turn credit-card-size tag antenna)
must be catered for requiring many of these “circular” transistors to be placed in parallel to get sufficiently many drain contacts in parallel (the emitter is made to have only one contact and is therefore at its smallest size). This area disadvantage lead to the development of other techniques discussed in Section 11.3.4 to reduce the effect of this parasitic vertical PNP.

When $V_{1a} > V_{1b}$, the opposite to the above discussion occurs.

### 11.3.4 Reducing the gain of the parasitic vertical PNP

Although it is termed vertical, the parasitic bipolar transistor also contains a lateral component. To reduce the gain of a parasitic bipolar, majority carriers in the emitter must be prevented from flowing to the base. Increasing the carrier concentration of the well reduces the base resistance but also reduces the gain of the bipolar, perhaps enough to not be an issue. Processes with differently doped wells usually exist with the lightest doped wells (highest gain parasitics) forming part of high voltage transistors which are usually required (essential for the over-voltage protection on the DC side) in the rectifier to prevent gate oxide damage, so unfortunately the more heavily doped well cannot be exploited. The base must therefore be made wider and/or the conducting path from the base to the node whose voltage allows the BE junction to be forward biased must have its conductance reduced. The base is made wider by making the well area larger which widens the lateral component of the parasitic transistor (the well depth cannot be changed to make the base wider as it is fixed on a particular process). The BE conducting path is made less conductive by placing resistance between it and $V_{DD}$. This latter method creates a lesser channel under the P-type MOSFETs due to the low-pass filtering properties of the gate-to-substrate capacitance and the well resistance but reduces the BE current in the “vertical” parasitic and therefore reduces the collector current. The value of the resistance was found by extracting a SPICE model for the vertical bipolar from fabricated structures and adding it into the netlist for simulations, in particular for AM detection at high excitation.

These parasitics are, annoyingly, rarely provided by a foundry in the form of SPICE models, so a first cut of any circuit design must always contain structures suitable for the parasitic parameters to be extracted. A “circular” MOSFET with a central drain can be modelled by a MOSFET with the same length but with a width equal to the average of the inner perimeter of the source and the outer perimeter of the drain. The areas and perimeters of the source and drain may be set to the values of the circular MOSFET.
A further way to reduce the collector current is by increasing the collector resistance which is provided by the length of the path through the P-substrate collector to the actual low resistance connection from the P+ implant to $V_{SS}$ via metal. This however means increasing the “diameter” of the P+ substrate guard ring around the P-type MOSFET’s N-well. This also raises the local substrate voltage above $V_{SS}$ in regions close to the N-well, and the separation of the well in question to other wells must be watched for lateral NPN (well-substrate-well) parasitics.

With reference to Figure 11.3, the size of M2 can be relatively small, with only small gains achieved by making it wider due to a PN junction “helper” diode D2 being in parallel with it and there being no problems associated with large voltages developing across this device during periods of high excitation. This configuration is actually that which is used in ESD protection devices and either the device can contribute to ESD protection or the ESD protection can contribute to rectification of this element although use of the latter in the absence of a dedicated rectifying element is protected by third party intellectual property (Waggoner 1999, Waggoner et al. 2001), with prior art of the technique with the presence of the rectifying element being held by the author. The minority carriers injected from the drain of M2, cathode of D2, into the substrate can be collected using a lateral bipolar transistor formed by placing an N-well guard ring around the N-type MOSFET which is connected to $V_{SS}$ via metal.

### 11.3.5 Explanation of guard rings

There are essentially two types of guard rings: those which are like-type implants in the substrate and well and those which are opposite types which form bipolar transistors to either convey carriers to where they belong (electrons to $V_{SS}$ and holes to $V_{DD}$) or to prevent other more detrimental parasitics from conducting. Figure 11.4 shows the basic guard rings used in an N-well process.

### 11.3.6 Placement of the elements

The main issue in the placement of the P-type and N-type is the separation of the wells (each P-type is placed in its own N-well) of the P-types and the well of the N-types’ guard ring. If the N-types and P-types are suitably separated the P-type N-well and the N-type N-well guard ring cannot form a lateral NPN which conducts should the vertical transistor associated with the P-type’s well conduct.
This is due to an increased series resistance connected to the lateral NPNs’ emitters. Figure 11.5 shows these parasitics as Q5 and Q6 when the wells are placed too close, while Figure 11.6 shows the situation when the wells are adequately separated with the resistors $R_{\text{sub,large}}$ preventing Q5 and Q6 from conducting. Although efforts have been made to prevent this vertical from conduction, a bit of conduction at the high extreme of the powering field can be tolerated providing the circuit’s voltage regulator is still the major controlling element of RF limiting, otherwise any communication in the form of AM modulation will be compressed and prevented from being detected.

Often the elements are separated in P-type N-type pairs at opposing sides of the chip, or the four individual elements are placed in the four corners of the chip. If this is not desirable or if suitable separation cannot be found economically when the elements are more closely spaced (a dual poly capacitor might be placed above the otherwise bare separation area) then a further N-well guard ring (or a semi-ring) is required between the P-substrate connection region surrounding the P-type N-well and the N-well guard ring of the N-types. This further guard ring forms the emitters of Q5 and Q6 and is connected to $V_{\text{DD}}$ as shown in Figure 11.7. Should the verticals Q1 and Q3 conduct and the voltage of the local substrate area around the P-type N-well (bases of Q5 and Q6) become positive with respect to
Figure 11.5. Circuit diagram of a CMOS rectifier including parasitics and guard rings.

$V_{SS}$, $V_{DD}$ to $V_{SS}$ pathways through Q5 and Q6 are no longer present since the collectors and emitters of Q5 and Q6 are connected with a low impedance via the metal connections connecting the guard rings (which form the collectors and emitters of Q5 and Q6) to $V_{DD}$.

Although there are issues with the parasitics associated with the P-type MOSFETs of this rectifier, the voltage drop between $V_{DD}$ and the positive cycle of the RF input is minimal and the efforts described in reducing the parasitic vertical bipolar’s gain and guarding the P-type from the N-type’s guard ring were only required for a 0.5 $\mu$m technology (and the same requirement is expected for smaller technologies).

### 11.4 The N-diode N-diode rectifier

In a process (generally those with smaller feature sizes) where the parasitic vertical bipolar associated with the well has high gain, avoiding the use of this well
as part of the rectifier results in a smaller rectifier (the elements may be larger but the overall structure including guard rings is smaller). The rectifier takes the form of the classical full-wave bridge rectifier with diode-connected MOSFETs (those in the substrate material) used as the “diodes” as shown as M2 and M4 in Figure 11.8.

The diodes M2 and M4 which conduct from input to $V_{SS}$ are the same as those in the previously discussed rectifier and therefore their operation and associated guard ring structures can be reviewed by consulting Section 11.3.
Figure 11.7. Circuit diagram of a CMOS rectifier including parasitics and guard rings with extra isolation well.

The diodes which conduct from input to \( V_{SS} \) are not free of design issues; first there is a threshold voltage increase of these devices due to body effect, and secondly there is a parasitic lateral NPN bipolar transistor with drain as emitter, substrate as base, and source as collector. The increased threshold voltage means that the gain of the MOSFET is reduced with a larger voltage drop between the positive RF cycle and \( V_{DD} \). This parasitic may conduct on the reverse bias cycle of the MOSFET diode in question. The lateral bipolar is not enhanced (Vittoz et al. 1985) in its performance due to the gate being tied to the drain in the rectifier (enhancement occurs when the channel is present) but still must be taken into account.

The following description outlines how parasitic conduction may occur, with nodes and devices being referred to illustrated in Figure 11.8. The voltage at \( l_a \) is negative with respect to \( V_{SS} \) which is approximately a “diode” drop voltage above \( l_a \). The node \( l_a \) is tied to the drain of \( M_1 \) and as this node is negative with respect to \( V_{SS} \) the PN junction is forward biased. The circuit path is completed by substrate resistance to the metallised substrate connection connected to \( V_{SS} \). As
electron current flows into the local substrate which forms the lateral NPN base, the source which is tied to $V_{DD}$ “collects” this electron current forming a conducting path between $l_a$ and $V_{DD}$ when $l_a$ is supposed to be connected to $V_{SS}$, thus clamping the RF.

The MOSFET gates of M1 and M3 are tied to the emitters, and as a result the gate-to-substrate voltage does not invert a channel and tends to push the electrons away from the surface so the pathway to the collector is longer, the effective base width being wider so the lateral NPN gain is reduced.

### 11.4.1 Layout considerations

In an effort to reduce the effect of the lateral NPNs of the “positive” diodes M1 and M3 in Figure 11.8, the MOSFETs associated with the “negative” diodes M2 and M4 are placed right next to the diodes M1 and M3 with the drains of each being shared. Here is where a greater gain of the negative diode MOSFET with respect to the implant-to-substrate diode is advantageous. During the negative cycle (where the parasitics of M1 may conduct) by enhancing the surface current through M3 the current from the shared drain to substrate is prevented, thus preventing the parasitic lateral NPN of M1 from conducting.
11.5 Electrostatic discharge protection

There are many types of electrostatic discharge (ESD) protection circuits (Beebe 1998, Amerasekera and Verwey 1992, Khurana et al. 1985) in use in microelectronics, some more suitable or effective than others for the various ways electronic circuitry can be configured to external devices. Chips for HF tags often only have two terminals for the antenna connection so techniques relying on the existence of a power supply are of little use. Chips may have more than two terminals, the additional terminals being used for testing of the digital circuitry or the memory but these terminals (which are often smaller to save chip area) are not handled by the tag assembler. A technique which effectively connects the two antenna terminals together during an ESD event is required.

11.5.1 Protecting the antenna terminals

The protection circuit designed by the author and used in the EM Marin 0.5 μm process consists of two N-type MOSFETs without the lightly doped drain (LDD) layer and without salicidation. Removal of the LDD layer or region predominately increases the level of current that may cause thermal runaway (damage) as the LDD generally has a lower junction depth than the drain region so under conduction there is a higher current concentration at the high electric field regions (thermal heating per unit volume is J.E). The “raw” unsalicided drain region adds some ballast resistance between the ESD event input terminal and the protection mechanism, which is particularly necessary when the MOSFETs are constructed from more than one gate (finger) region (as is the case for parallel devices), as it allows the multiple devices to conduct, otherwise once one path conducts first, due to it having slightly better conduction due to process imperfections, that path would dominate and the lower voltage that exists once conduction occurs would prevent the other parallel devices from conducting.

The two MOSFETs have their gates tied to ground through a resistance whose role will be explained in a further paragraph. Their drains are connected to the antenna input terminals and their sources connected to the chip VSS. Wide metal is used for these drain and source connections as up to 1.5 A of peak current may flow in a 4 kV human body ESD event. The human body model consists of a 100 pF capacitor, charged to a voltage and discharged through a 1.5 kΩ resistor. Figure 11.9 shows this arrangement including parasitic lateral NPN bipolar transistors.
The operation will be described assuming a positive ESD event with la positive with respect to lb. An ESD event is a sharply (1 to 10 ns) rising voltage waveform which lasts around 100 ns. As the voltage on la rises to what is usually denoted $V_{bdDS}$, the reverse-biased drain-to-substrate junction of M1 (shown as the collector-to-base junction of Q1) starts to inject carriers (holes) into the P-substrate due to the formation of electron-hole pairs through impact ionisation (II), with the return path to lb formed via the forward-biased P-substrate-to-drain diode and the diode-connected transistor M2 ($V_{SS}$ connection acting as the drain in this case). These II-holes pass to the substrate connection as a result of the finite resistance between the substrate near the drain and the substrate connection to $V_{SS}$. A positive voltage is created under the channel (the base of Q1). Eventually the drain voltage of M1 rises to a level known as the snap-back trigger voltage (Zhang et al. 1996) where the base-to-emitter voltage of Q1 reaches around 0.6 V which forward biases Q1 on, and collector current starts to flow between la and $V_{SS}$ which lowers the voltage at la to a level known as the snap-back voltage. With the ESD input event still rising in voltage, the current through Q1 increases as does the voltage at la due to a finite resistance in the conducting path of Q1.

In the theory of operation of such a protection device M1 (M2 is considered as a forward-biased diode to complete the circuit), there exists a second trigger voltage which signals the start of thermal runaway. This is the point where the Joule heating of the drain-to-substrate junction has caused the intrinsic concentration of carriers to reach the same concentration as the doped region(s), with the result that the drain-to-substrate junction is no longer a reverse-biased junction and the current continues to rise causing further heating and a further intrinsic carrier concentration increase. This second trigger voltage is thus required to be avoided, and the widths of the transistors (M1 and M2) must be suitably sized such that
the desired ESD event (that which protection from is afforded) is over before the second voltage is reached.

MOSFETs conduct more quickly than the diodes associated with their regions, so a technique to get a bit of current flowing in the drain to enhance the onset of impact ionisation is what is known as “gate bounce”, and is shown in Figure 11.10. The gates of the protection devices are tied to the sources via resistances $R_{g1}$ and $R_{g2}$, which in conjunction with the drain-to-gate capacitance form RC circuits which initially place a positive voltage on the gate during the rise of the corresponding drain voltage. This turns the MOSFET on, and then the gate discharges back to zero with a time dependent on the RC time constant and the actual shape of the ESD event. The effect is to lower the snap-back trigger voltage, with a $10 \, k\Omega$ resistance lowering a $250 \, \mu m$ wide (0.5 $\mu m$ process) transistor’s trigger points by around 1 V.

The effect on chip input impedance of the introduction of the shunt diode-connected MOSFETs M1 and M2 as the ESD protection is minimal. The leakage at low excitations is negligible (the protection devices actually contribute to rectification) and the added input capacitance though process and voltage dependant is of the order of 1 pF, where the tag’s total capacitance is typically around 15 pF or more. As a consequence similar guard rings to those around the diode-connected N-type transistors need to be placed around the protection devices. A 20 % drift in the value of capacitance of an element which contributes only 7 % to the total capacitance results in a 1.4 % tolerance. This tolerance on chip input capacitance can be
considered as purely process dependent as chips are often trimmed for correct input capacitance for low excitation. At high excitation where voltage dependence might play a role, the chip is shunting 100000% of the power the circuitry is consuming, so the tag has a low Q so 1 pF of detuning has no discernable effect on the resonant frequency of the tuned circuit.

11.6 The N-diode N-switch rectifier

During the design of the TAGSYS C320, the analogue circuits of which were designed by the author, it was found that carriers injected into the substrate from the rectifier shown in Figure 11.8 were finding their way into the N-well resistor associated with a current reference. The rectifier was modified by changing the diode-connected N-type MOSFETs connected to \( V_{\text{SS}} \) into N-type switches as shown in Figure 11.11.

While this resulted in a slightly less-efficient rectifier at low RF excitation, the clamping action of the MOSFET switches reduced the level of carrier injection into the substrate at high RF excitation.

The circuit operates similarly to the rectifier described in Section 11.4 with the exception that instead of MOSFET diodes shunting the substrate diodes between

![Figure 11.11. Circuit diagram of a N-diode N-switch rectifier.](image)
the input terminals and \( V_{SS} \) as the input RF voltage increases, MOSFET switches provided the shunt path.

### 11.7 Summary

HF rectifiers have been implemented in 4 chips of which the analogue circuits were designed by the author.

The rectifier shown in Figure 11.2 was successfully used in the ISD 72128 and TAGSYS C220 using a Chartered Semiconductor 0.8 \( \mu \)m process.

The TAGSYS C310 and C320 HF chips were fabricated in an EM Marin 0.5 \( \mu \)m process. Due to the high gain of the parasitic vertical bipolar associated with the N-well, P-type MOSFETs as shown in Figure 11.2 were not used. Instead the rectifier shown in Figure 11.8 was used for the TAGSYS C310 chip, and due to placements of sensitive devices near to the rectifier in the TAGSYS C320 chip the rectifier shown in Figure 11.11 was used.
Chapter 12

Passive Shunt Regulators

This chapter describes shunt voltage regulators with the following features: they are fully self-contained requiring no other inputs from other circuits; they are fast acting to prevent chip damage in the case where a strong excitation field is switched on; and they have a built in hysteresis so that dips in the excitation field may be detected even under strong excitation when the regulator is heavily clamping the supply voltage. The regulators have been used successfully in a number of commercial chips.
12.1 Introduction

The tag receiver circuitry is that which receives signals from the reader in the form of carrier modulation to provide commands or data to the tag. The work in this chapter has been influenced by market realities in two main ways: in choosing communication methods similar to those used by standards groups and hence large volume RFID tag consumers; and by exploiting a feature of a power regulator which uses a method different from those where third party patents are held. The receiver is divided into two functional sections, a modulation detector, and a shunt voltage regulator on the DC side of the rectifier. Mention of the receiver and in particular the modulation detector is necessary as that detector responds to small dips in supply voltage which occur when the excitation field is amplitude modulated, therefore the design of a shunt voltage regulator is closely linked to modulation detection.

12.2 Modulation detectors

12.2.1 The AM detector

An AM detector was chosen due to its almost universal use in tag communication specified by standards bodies, primarily due to simple implementation in the reader circuitry. The AM detector chosen, operates by comparing a first reference voltage, which varies with the instantaneous supply voltage, to a second which varies with the time average of the supply voltage. Other classical forms of detector actually detect the AM carried on the AC waveform at the antenna. The reasons and benefits for not using that classical approach were:

- larger modulation indices are required at the rectifier input to maintain a detectable variation in conditions of RF limiting and;
- due to the RF limiting circuit being on the DC side of the rectifier, circuitry to regulate the supply voltage can be simple or avoided altogether. When using a 0.8 μm feature size digital process or an analogue process, extreme over-voltage protection of the MOSFETs when the tag is in high fields is not required.

Features of the design are low-current-consumption voltage references and a low-current-consumption comparator. If a comparator is constructed from an operational transconductance amplifier (OTA) which has a differential voltage input
but a current as an output, the single output gain stage has good immunity to parasitic feedback paths due either to poor layout or the driving of capacitive loads, and a dedicated feedback capacitor for frequency compensation as often used in an operational amplifier is not required thus saving space.

### 12.2.2 The voltage comparator

A first reference voltage is constructed by using a constant current sink and a diode-connected P-type transistor between $V_{DD}$ and the current sink. A second reference voltage is constructed using a second “diode” with similar geometry as the first, but the current sink is made by using a transistor with the same length as the first current sink but wider in order to have an increased current. Both current sinks have their associated gates connected to the same bias voltage such that the relative currents will be proportional to the ratio of the widths. In this way the first reference voltage will always be higher than the second, due to the increased voltage drop across the second diode which has a larger current flowing through it.

### 12.2.3 Choosing the nominal current

The nominal current for the reference with the lowest magnitude of current, is chosen by consideration of the transistor lengths to be used for current references throughout the design and the value of current in the current reference that is to be mirrored. It is of course desirable to use the lowest value of current that will keep the sink transistor in saturation for all operating conditions. The lengths for sinks and sources in this work were chosen by consideration of the longest device for which the SPICE model supplied by the foundry is known to give accurate results.

Deviation from the maximum recommended length, or rather from that which is known to be correctly modelled, requires fabrication and measurement of the characteristics. As it is difficult, due to noise inductively picked up by probing wires, to measure the characteristics of a transistor with currents of nanoamperes, a reliable technique is to fabricate a circuit which produces a reference voltage connected to a simple differential comparator such that a second externally applied reference voltage is used to check the internal one (Alsarawi and Cole 1995). The external voltage required to change the state of the comparator versus supply voltage, process parameters, and temperature can be recorded and checked.
against the SPICE model and modifications to the model can be performed to match the empirical observations.

Using such a technique, a transistor with a length around twice that of the nominal maximum has been shown to work well.

The transistor is desired to be long such that any process length variations form a small percentage error compared to the overall length. Leakage from the drains to surrounding diffusions must be considered where low current values are desired. The current through the sink or source must be dominant with respect to any leakage. Critical transistors can be surrounded by the diffusion type which is used to connect its substrate or well to the supply, to provide a stable path for any leakage. Leakage to diffusions which change their voltage levels results in unpredictable circuit behaviour or in extreme cases latchup.

The two reference voltages are separated by enough voltage to protect against any noise on the supply as a result of minor modulations of the energising carrier and other electromagnetically coupled noise. It is believed that only after the measurement of noise in industrial environments that the minimum amount of noise margin can be estimated. Electric motors and switched-mode power supplies are amongst the worst offenders and are always encountered in industry. With larger AM indices the difference between the two reference voltages may be increased to provide larger noise margin.

The lower reference voltage is low-pass filtered and then compared with the higher unfiltered voltage. When the supply suddenly dips as the result of momentary loss (100 % AM) or reduction in amplitude (< 100 % AM) of the energising field, the higher reference voltage has an instantaneous value less than the time average of the lower filtered voltage and this condition produces a level change at the output of the comparator.

12.2.4 A low-pass filter

An active low-pass filter consists of a differential pair with active loads, but unlike an OTA, no second output stage is required. The single ended output and the gate (positive input of the differential pair) of the transistor whose drain shares this output node are connected together and further connected to a shunt capacitor to $V_{SS}$. The other gate of the differential pair (negative input) is connected to a reference voltage.
At power-up the output is low which causes the “negative” input transistor to be on thus charging the capacitor until the voltage equals the input where an equilibrium is reached. Should the input drop suddenly, the “positive” input transistor conducts more than the “negative” input transistor which causes more current to flow through its active load which in turn, via current mirror action, places the load transistor of the “negative” side in a higher conduction state which starts to discharge the capacitor. After a decay time, the voltage on the capacitor would reach a new equilibrium, but for the AM receiver the time constant is set such that the capacitor voltage doesn’t change much for the duration of an AM pulse in order for the circuit to be ready for a subsequent AM pulse with the input returning to and again starting from the first pulse’s initial conditions. The time constant is short enough to follow the slower changes in circuit voltages due to a tag moving through the energising field, so that communication can occur to a moving tag.

12.2.5 A voltage-pulse-detect circuit

An example of a voltage-pulse-detect circuit designed by the author which includes a comparator and a low-pass filter is shown in Figure 12.1. The nodes opd and stop are control inputs: opd is short form for “operational-power-detect”, a signal for when sufficient voltage to operate chip circuitry exists; and stop is a signal which “stops” the detection of pulses while the tag is itself modulating.

12.3 The regulator

The regulator, shown in Figure 12.2, prevents circuit damage by limiting the large voltages that would otherwise develop when the tag antenna is closely coupled to the reader antenna. The shunt regulator clamps the supply at a safe maximum but not without affecting the tag’s ability to convert electromagnetic field to chip supply voltage, or the tag’s quality factor (Q) as the shunt regulator increases chip current and reduces the chip’s input resistance.

The feedback dynamics of the regulator must be investigated to prevent oscillation during modulation of the energising carrier. The voltage delivered to the chip is proportional to the tag Q, if the voltage sharply rises, perhaps due to tag movement or an increase in the powering field (both intentional and unintentional), the regulator increases the conductance between the supply and ground presenting a
Figure 12.1. The voltage-pulse-detect circuit.
lower impedance to the antenna which lowers the tag $Q$ and subsequently converts less of the electromagnetic field into supply voltage, to which the regulator responds by decreasing the conductance across the supply.

Two operational modes of the regulator are of interest; one in which the regulator just regulates, tracking any changes in the field; and a second in which the action of regulator lags behind any drops or rises in the field. The former is used when the tag is modulating, where it is possible that increased supply voltage may develop due to a possible shift in the resonant frequency of the tag. The latter action is useful in the detection of AM communication from the reader when the tag is close to the reader antenna and the regulator is dissipating upward of 30 dB more power than the tag electronics actually require for operation. During the periods of AM from the reader, the regulator allows the supply voltage to vary with the energising field, in effect providing less regulation. The AM commonly encountered in an RFID system is in the form of dips of the energising signal, so no over-voltage situations occur with the lagging action of the regulator.

For communication between the reader and the tag various mixes of half-duplex and full-duplex methods can be used, each with their own merits. One method considered is phase modulation (PM) in the forward link (reader to tag) and AM
(really a mix of AM and PM) in the return link (tag to reader). The use of AM (even shallow or small index AM) in the forward link for full-duplex reader communication poses a limitation in that the small amplitude tag reply must be recovered out of the larger dips in the carrier, and the associated transients in the reader’s receiver circuitry.

The use of AM in the forward link for full-duplex tag communication is also a problem. During tag modulation: the RF at the antenna varies in amplitude presenting difficulties for a classical detector; and for a detector of the type used in this work, which looks for supply variations, the supply voltage varies. The forward modulation must have a large AM index to be separated from the tag’s own modulation, which presents the problems of requiring a larger tag supply reservoir and larger amplitude sidebands radiating from the reader which may infringe EMC regulations.

When the regulator circuit is not operating and the field drops by \( \approx 20\% \) (\( \approx 10\% \) AM index), so too does the supply voltage.

When a simple regulator is operating (i.e. limiting the supply voltage), if the field drops the load required between the supply terminals to maintain a safe operating voltage becomes less, so the circuit eases its clamping effect with the resulting supply voltage basically remaining at the level prior to the field drop. Of course the circuit cannot react instantaneously (as in the lagging regulator), and depending on the duration and depth of the field drop and amount of reservoir capacitance the supply voltage may drop but at a reduced level as compared to that of the energising field. This reduction in level is referred to as AM compression.

When a tag is subjected to a field of 5 A/m the compression effect is so great that there is virtually no dip in supply voltage. For example, when the steady state field strength is 30 dB higher than the minimum required for circuit operation, during an 18 % dip (the amount of dip for a 10 % AM index) in field strength, the field strength is still 28.3 dB higher than the minimum required, thus a simple regulator would still be shunting much more current than the chip consumes and the supply voltage would not dip along with the field strength.

Detecting shallow AM is one area where the author has made significant contribution to the RFID industry’s knowledge, within the chosen shunt regulator architecture. Some designs, such as Electra/Gemplus STM chip and EM Marin ISO15693 which have been tested directly, suffer from AM compression or the symptom that “it works fine but not close to the antenna”.
When a regulator with a lag feature is operating, if the field drops the slow response to voltage variations maintains the same value of conductance across the supply which kept the voltage at a safe level, resulting in a temporary over-clamped condition which causes the supply voltage to drop. The AM pulse width and depth, the amount of capacitive storage on the chip, and the time constant of the regulator all contribute to the nature of the voltage drop. Generally it is desired to have the time constant of the regulator to be larger than the pulse width so that the over-clamped condition lasts long enough to produce a drop in the supply with a sharp leading edge even when storage capacitance is present.

Start-up conditions can be quite severe in cases where the tag is close to the reader antenna and the energising field is suddenly applied. If the circuit does not react quickly enough the chip will be subjected to an over-voltage condition both in terms of supply voltage and input voltage which may damage transistors or capacitors of the circuit. ESD devices do not afford protection in this case as the ESD event has a sharper rise (dV/dt) and comes from a higher impedance source. This is another area where classical regulator designs fail, for example if they rely on current mirrors for reference voltages to be set up they cannot activate quickly enough to prevent this “snap-on” stress condition and oxide breakdown. This is the reason that a totally independent limiter design has been chosen.

If a lagging regulator is to be solely used, it must still react quickly enough to protect the circuit against power-up stress.

### 12.4 Regulator design

The regulator design starts with finding the lower operating point at which it starts to shunt current and the upper operating point at which the tag with the largest antenna to be used is immersed in the highest amplitude field. The lower limit is typically set at the voltage at which the process is rated, that normally being where all circuit elements work correctly (read voltage for EEPROM usually sets this lower limit). For voltages up to this lower limit the regulator should only shunt minimal current so that the tag may operate at maximum range.

The upper limit may be found from experiment or modelling of the largest proposed tag antenna and the rectifier to be used. The design is linked somewhat iteratively to that of the rectifier as there is a balance between the maximum shunt current of the regulator and the output impedance of the rectifier under this maximum condition.
In the maximum-field condition the voltage developed at the tag’s antenna terminals must be below both the working voltage of the oxides of any RF tuning capacitors, and the maximum drain-to-gate voltage in any transistors connected to the antenna terminals.

The International Standards Organisation (ISO) currently requires a tag to survive a 12 A/m field when a credit-card-size antenna is used, however it is wise to allow the tag to survive this field with the largest antenna the chip is conceived to be connected to.

12.4.1 Maximum-stress measurements

The procedure listed below to perform maximum-stress measurements was followed.

1. Set up a 12 A/m field by one of the following methods:
   - providing the correct input excitation to a calibrated transmitter antenna; or
   - adjusting the excitation to an antenna whose field is measured by a calibrated antenna or field probe; or
   - calculating the field of a wire coil or loop and applying an appropriate excitation.

2. Select the largest coil antenna that is to be used.

3. Connect a high impedance oscilloscope probe across the coil (tag coils are typically parallel resonant).

4. Connect the coil to the chip (a version which has less capacitance than the target internal value by an amount at least equivalent to that of the oscilloscope probe). If no chip is available it may be replaced by a suitable rectifier and resistor combination. A resistor value equivalent to the power-on reset (POR) value of the chip supply divided by the current at that supply value is a good approximation. A typical chip will have a non-linear rise in current with supply voltage and a linear approximation will result in a higher than expected rise in supply voltage with excitation, but a design which copes with this supply voltage rise provides a margin of safety.
5. Adjust the low-power resonant frequency (such that the chip does not activate) to the carrier frequency, with the probe connected across the coil by use of an adjustable trimmer capacitor across the coil. This may not be the final operating frequency of the tag but it will be very close to the maximum stress condition. Again use a rectifier and resistor arrangement if a chip is not available.

6. Connect a variable resistance across the chip’s supply or equivalent. This resistance will be reduced to load the test tag such that the coil voltage is within safe levels.

7. Gradually immerse the tag in the field so as not to go over voltage, while adjusting the resistance across the supply to keep the peak voltage across the coil at the maximum safe value. The supply voltage is recorded. The value of the resistance at full field is that which must be provided by the shunt regulator when the chip supply voltage is at the recorded value.

8. Should the supply voltage be higher than desired, additional shunt current will be required with a favourable side effect of reducing the RF stress, or the rectifier’s impedance may be increased (smaller size) along with an appropriate increase in shunt current. The ratio which yields the smallest overall chip area will vary from process to process.

9. Should the supply voltage be lower than desired the rectifier’s impedance will need to be reduced (larger size), again with a favourable reduction of RF stress, or the rectifier’s impedance will need to be reduced along with an appropriate reduction in shunt current. Again the solution should be chosen to give the smallest chip area.

12.4.2 The basic shunt regulator

Figure 12.2 shows the basic shunt regulator. This regulator works well with larger geometry processes (such as 0.8 $\mu$m) as there is plenty of “head room” in terms of voltage levels that can be safely achieved. The layout of the regulator of Figure 12.2 is shown in Figure 12.3.

A diode string using diode-connected MOSFETs was used to set up a series of reference voltages that are linked to the threshold voltage of the transistors.

As is typical in I/O circuitry, only the MOSFET type which occurs in the substrate was chosen to eliminate parasitic BJTs which form between wells and other
diffusion areas including other wells. In the P-substrate process this means only N-type MOSFETs will be utilised in the RF limiter or voltage regulator.

As the threshold voltage of the process varies, the diode reference levels change but so too does the operation of the other transistors in the chip as MOSFET oxides track each other on a particular wafer. This means that a relative approach to reference voltages can not only safely be utilised but it is often required when the difference in the antenna terminal voltages between the two extreme operating points is small.

The last diode in the string is connected to a “resistor” M5 in Figure 12.2. The voltage across the resistor is effectively 0 V until the supply reaches the stacked voltage of the diodes at which point current starts to flow through the resistor and the voltage across the resistor rises and will continue to rise with the supply. The resistor voltage drop is connected to the gate of a large N-type transistor whose drain and source are connected across the supply. This transistor is sized so as to provide the required amount of limiting or equivalent resistance at the gate voltage that results from the supply voltage equalling that when the tag is excited by the maximum field, as well as maintaining negligible current drain at power-on reset (POR).
Iteration of values will yield the final combination of geometries for the “diodes”, the “resistor” and the shunt transistor.

A starting point for the diodes which results in a “unit” device which exhibits the minimum change over process and voltage variations can be found from the following procedure. The current through a MOSFET is given as:

\[ I_{ds} = \beta \left( (V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right) \]  

(12.1)

Assume an N-type MOSFET with the source and bulk set to 0 V. Set \( V_{ds} \) to a low positive value e.g. 0.1 V. Plot \( I_{ds} \) vs. \( V_{gs} \) for \( V_{gs} \geq 0 \) and measure the final slope \( m \) when \( V_{gs} \) is increased enough to display a clear trend of linearly increasing \( I_{ds} \). For large \( V_{gs} \), \( V_{gs} - V_t > V_{ds} \) and the second-order term becomes small (0.005 in this example) in comparison with \( 0.1(V_{gs} - V_t) \) and thus can be ignored resulting in the slope \( m \) approximating \( \beta \times V_{ds} \) (0.1\( \beta \) in this example) in Equation 12.1. Thus the region of maximum slope projected back to the negative \( I_{ds} \) axis (the y-intercept \( c \)) will equal \(-\beta \times V_{ds} \times V_t \) (0.1\( \beta \)\( V_t \) in this example), and hence yielding \( V_t \) from \(-c/m\).

This procedure is repeated for various width to length ratios over the process corners and temperature to yield for a chosen width, for example, the smallest length which results in the smallest change in threshold voltage over the testing matrix. So if a high gain (wide) analogue transistor or a “diode” with a low forward voltage is required a “wide length” will be found. The opposite case of a low gain (narrow) analogue transistor or a “diode” with a high forward voltage will yield a larger in value “narrow length”. These high and low forward voltage drop diodes form “unitary” devices.

Using various combinations of these “unitary” devices, a stepped series of reference voltages may be formed, with each voltage step being due to the voltage drop across a “unitary device”. Although the actual voltage levels may change from wafer to wafer, a certain string of narrow diodes will always have a higher voltage drop than a string with the same number and configuration of wide devices. The philosophy is that if the weakest device has sufficient supply voltage to operate correctly, then a stronger device will also. In another way, if process variations act upon the regulator to clamp at a lower value then the same process variations cause an inverter to operate correctly at the lower supply voltage (providing the regulator is not over-clamped for typical conditions).

This regulator is the tracking type. It is useful in so-called field-programmable devices where tags will only be programmed under controlled conditions allowing
lower field strengths or larger AM indices (providing the field is sufficient to run
the programming circuitry) to be used, avoiding the AM compression effect. It is
also a mode of operation useful when tags may experience increased excitation in
a replying mode due to their modulation method causing them to shift their reso-
nance in the modulated state closer to the carrier than when in the unmodulated
state.

12.4.3 A lagging regulator with a capacitor

Using the regulator of Figure 12.2 as the foundation, if the voltage on the gate of
the large shunt transistor was maintained momentarily, the regulator would be in
an over-clamped situation resulting in the desired behaviour of deepening com-
pressed AM dips. Figure 12.4 shows an example of a regulator with a capacitor
storage node.

With reference to Figure 12.4, moving the large shunt transistor’s (M8) tap point
up in voltage (to the drain of M4), and then back down with another diode-
connected transistor (M6), maintains the maximum voltage level while adding
the desired delay. Another diode (M7) is connected across the dropping diode,
but with reverse polarity, forming a “back-to-back” configuration which increases
the leakage path to the shunt transistor’s (M8) gate and provides a bottom limit to the drop in supply voltage during carrier dips. The sizing of these diodes (M6 and M7) is chosen to give enough dip at maximum energisation and not too much dip at POR.

If the gate of the shunt transistor (M8) does not have sufficient capacitance to provide the necessary charge storage, then additional capacitance is added between its gate and VSS. This may also be necessary if the gate-to-drain capacitance is too high as the result of a transistor layout which uses multiple gate fingers to reduce chip area.

### 12.4.4 Step-input stability

The step-excitation stability must be checked so the circuit does not exhibit either excessive clamping or oscillation during sudden application of the carrier.

Excessive clamping occurs if the gate-to-drain capacitance is large enough for the gate to be pulled high as the supply goes high during the input step, bypassing the charging diode(s). This effect is known as “gate bounce” and can be exploited for ESD protection, but alas is not desirable here. The gate reaches a higher voltage than it would in normal operation (leakage is not enough to counteract the effect of the step input acting through the drain-to-gate capacitance).

Oscillation after a step RF input may occur if the delayed-action time constant is too high. The sudden application of RF in this condition, causes the supply to overshoot its clamped value, then as the controlling voltage catches up it reaches a value corresponding to a falling but still over-voltage supply which causes excessive clamping. The circuit then continues to flip between under-clamped and over-clamped situations, with each cycle being less extreme as the previous (damped oscillation) and the circuit will eventually settle but in the meantime the chip is not ready for AM communication and the initial under-clamped condition may have been long enough to destroy device oxides.

The step input should be investigated at “even” steps (in dB terms) from POR to maximum field as the oscillation may not only occur at the higher excitation levels.

A first approach to solve the oscillation problem was to make the time constant for the lagging operation asymmetrical. The controlling node was made to charge quickly, i.e. it protects the chip against step RF inputs, but discharge slowly, i.e. it avoids an over-clamped condition during dips in the carrier. The asymmetry
can be implemented by the size ratio of the back-to-back diodes (M6 and M7 of Figure 12.4), or by using identical geometries for the diodes but connecting them to different tap levels in the diode string (the charging diode at a higher tap level than that of the discharging diode).

12.4.5 A lagging regulator without a capacitor

In processes without the necessary head room, i.e. when the forward voltage drop of a wide diode-connected transistor is large compared to the voltage variations between POR and the fully clamped supply at maximum excitation, dropping the supply by the forward voltage drop of a wide diode-connected transistor during an RF dip may not be acceptable. Experiment has shown this to be the case with feature sizes less than 0.8 µm. When these smaller geometries are used, the voltage difference between activation and limiting is reduced (to protect the thinner oxides used throughout the smaller geometry process) so a different regulator was developed which still promoted supply voltage dips during RF pulses, but with shallower and more-controlled dips over the excitation range.

The regulator design shown in Figure 12.5 started with a similar diode string to set the point at which clamping will start, but instead of using a capacitor as a charge storage node (as shown in Figure 12.4), a current mirror type arrangement using two additional transistors M4 and M7 was developed to control the gate voltage of the clamping transistor M8. The current source M6 charges the gate of M8, while at the same time the current sink M7 discharges the gate of M8, normally keeping the gate voltage at an equilibrium. During an RF pulse the ratio of the currents that charge and discharge the gate of the clamping transistor M8 change which causes the regulator to temporarily over-clamp which results in a dip in the supply voltage.

The mirror stages are arranged such that the charging current is derived from the bias stage via a 1:1 geometry ratio, whereas the discharging current is derived using a 1:20 geometry ratio such that less current is in the mirror stage. This ratio difference is what provides the lagging features, the voltage on the gate of the clamping transistor is able to rise quickly to prevent over-voltage of the supply, but is only able to fall slowly, thus during a momentary loss or reduction in energisation the circuit is over-clamped providing the desired fall in supply voltage.
Should the energisation fall due to tag movement the circuit is able to adapt in time because the rate of change in excitation is small compared to that which occurs during a dip. Typically, the shallowest dips are of about 10 % AM index (or 18 % dip depth) in amplitude and 6.44 µs fall time from 0 to 100 % (the slowest fall time allowed by ISO18000). The author has been directly involved in this standard since 1999 and the parameters finally published are a compromise from many manufacturers between cheap reader and tag construction, and system performance.

Modulation Index is $(a - b)/(a + b)$, and Modulation Depth is $(a - b)/a$, where $a$ is the normal steady state amplitude and $b$ is the level at which the amplitude reduces to for the most part during a dip (there may be momentary undershoot of $b$ for reduction in spectral components). So for each volt developed in the coil from the initial steady state carrier, a shallow dip has a rate of change of 28 mV/µs. Movement of a tag through a field is rarely more than 160 kph or 44.4 m/s (a car on a highway) for a far-field system and 10 kph or 2.8 m/s (a fork lift in a wharehouse) for a near-field system. Based on a 0.1 m movement through the field, the speeds mentioned give the tag comparable rates of change of 0.22 mV/µs for far field, and 0.025 mV/µs for near field, both of which are considerably slower than the rate of change for the slowest dip.
12.5 Summary

Shunt regulators have been implemented in 4 chips of which the analogue circuits were designed by the author.

The regulator shown in Figure 12.2 was successfully used in the ISD 72128 and TAGSYS C220 using a Chartered Semiconductor 0.8 μm process. These chips were field-programmable only which means they were not required to detect shallow AM while under large excitation. The oxides in the process allowed around 18 V peak voltages.

The regulator shown in Figure 12.5 was successfully used in the TAGSYS C310 and C320 HF chips using an EM Marin 0.5 μm process. These chips were at the time a subset of ISO18000M3, hence they were shown to survive a magnetic field of 12 A/m when connected to a credit-card-size loop antenna. These chips were reader-talks-first (RTF) and were therefore required to detect shallow AM while under excitation of 5 A/m. The oxides in the process allowed around 10 V peak voltages.
When circuit functionalities are required to be different depending on whether a chip is on-wafer or off-wafer, some kind of switch is required that changes state when the wafer is sawn. The on-wafer detector described in this chapter carries one logical bit of information with one state representing the integrated circuit being on a wafer (before dicing or sawing), and the other state representing the integrated circuit being off of a wafer (after dicing or sawing). The detector has been successfully incorporated into two commercial chips.
Chapter 13  A Zero-Power On-Wafer Detector 177

Figure 13.1. General schematic of the wafer detect circuit.

13.1 Introduction

It is a common technique to place wires, pads and even circuitry for on-wafer testing purposes in the wafer scribe region which is otherwise unused and wasted when the integrated circuits are diced or sawn into individual chips. The technique used in our on-wafer detector is that of a wire (represented as R1 in Figure 13.1) which passes from the circuit region into the scribe region and back to the circuit region, forming a conductive loop of a material different from the materials used in the chip periphery seal ring\(^8\), or in the case where the material is one of those used in the seal ring, the seal ring is modified at the areas of intersection with the loop such that the loop is not electrically connected to the seal ring.

Simple resistive pull-down (or pull-up) structures have been proposed by chip foundries to achieve two distinct DC levels representing on-wafer and off-wafer integrated circuit conditions when the integrated circuit is powered. The drawback of this type of structure is that due to process dependency the true integrated

\(^8\)A protection ring around a chip in order for multiple chips to be tested in parallel on-wafer without influence from neighbouring chips. In CMOS circuits it is usually formed by a ring of diffusion of the same type as the substrate with contacts to metal layers stacked above to form a low resistance path around the chip.
circuit power consumption cannot be measured without the measurement needing to be corrected for the current draw of any resistive, or current source or sink elements which are themselves process dependent.

The key property of the implementation presented here is that the on-wafer detector has zero power consumption (other than leakage). This allows the true power consumption of the integrated circuit to be measured while on-wafer testing is performed.

13.2 Circuit operation

Figure 13.1 is a representative circuit of the on-wafer detector, with a P-type substrate chosen for illustrative purposes. The circuit can be implemented equally by the use of N-type or insulator-type substrates, with the correct device polarity exchange as deemed appropriate. In Figure 13.1 the capacitor C1 is made larger than capacitor C2. These capacitors may not be require to be added explicitly to the circuit, they may be provided by the respective drain-to-substrate capacitances of transistors M1 and M3.

Upon power-up with R1 present, nodes a and b are pulled toward the positive supply rail which causes node c to be pulled to the zero rail by the inverter INV which causes nodes a and b to be reinforced to the positive supply rail by transistor M1. Thus when the chip is on wafer node c is in the low logic state.

Upon power-up with R1 removed (destroyed by dicing or sawing) the nodes a and b may individually be floating, or shorted to the substrate if the metal in the scribe lane melts into the substrate during sawing. Node b is initially low due either to a substrate short or to capacitor C2, which causes node c to be initially high which reinforces node b low by transistor M3. If node a is initially low due to a substrate short, node c being high reinforces that state by transistor M2, or if node a is initially high due to capacitor C2, node c forces node a to the low state after charging capacitor C1 again by transistor M2. Thus when the chip is off-wafer node c is in the high logic state.

Transistor M2 is included to force node a to the zero supply rail in the case that node a is shorted to the substrate, preventing any substrate current injection.

The circuit may be modified to perform a pre-test and post-test detector function. In Figure 13.1, R1 may be replaced by a fusible link or a storage device fabricated in a known state, such that before testing or during the first test stage the detector
is in one state, and after testing or during a second test stage the detector is in the opposite state achieved by laser cutting the fusible link between tests or changing the state of the storage device during the first test stage.

### 13.3 Specific implementation

The detector arrangement as shown in Figure 13.2 was fabricated on EM Marin’s 0.5 μm digital process. The circuit requires that LOOPA be connected to LOOPB (with a poly loop) when the circuit is “on-wafer” or “not cut” which results in an output of $C = 0$ which is then buffered for a fan-out of 3, so that the circuit may be isolated from the logic it is to drive, resulting in an output of $W\_CUT = 0$.

The initial condition that LOOPA (and subsequently LOOPB as the two nodes are joined by a poly loop prior to dicing) is high with the poly loop present is ensured by the addition of a capacitance between node C and $V_{SS}$ which is implemented by the gate-to-source (gate-to-substrate) capacitances of MNH18 and MNH20. Thus node C (which has twice the capacitance to $V_{SS}$ as LOOPB and as such will be the last node to be dragged towards $V_{DD}$) is initially 0, and as $V_{DD}$ ramps up, LOOPA goes towards $V_{DD}$, as does LOOPB through the loop connection, which
charges the gate capacitance of MNH19 and turns MNH19 on which reinforces the 0 condition at node C, and output $W_{\text{CUT}} = 0$.

When the loop is cut, the gate capacitance of MNH19 holds LOOPB at 0 which sends node C towards $V_{\text{DD}}$ which charges the gate capacitances of MNH18 and MNH20 and turns on MNH18 which reinforces the 0 condition on LOOPB, and output $W_{\text{CUT}} = 1$. (LOOPA is sent to 0 due to node C going to $V_{\text{DD}}$.)

Each of MNH18, MNH19, and MNH20 have a gate capacitance of 408 fF to $V_{\text{SS}}$.

### 13.4 Verification of the circuit

SPICE analysis of the circuit was performed by applying a 10 $\mu$s ramp to 3 V through the chip rectifiers, emulating the application of a testing voltage by a wafer prober (the TAGSYS C310 and C320 HF chips were to only have 2 antenna pads).

Absolute worst-case parasitics were applied to nodes as follows:

- adding to the appropriate nodes the worst-case parasitic capacitance for all interconnects;
- adding the 3 gates that normally are connected to output $W_{\text{CUT}}$ to un-buffered node C;
- adding 1 pF to output $W_{\text{CUT}}$ which was $90 \times$ the load of the required fan-out; and
- using the slow and fast parameters of the process.

Figure 13.3 shows the circuit behaviour with the scribe lane loop connected. There are 2 traces for each node which represent the slow and fast parameters of the process.

Figure 13.4 shows the circuit behaviour with the scribe lane loop opened by sawing.

Figure 13.5 shows the circuit behaviour with the scribe lane loop broken but node LOOPA shorted to $V_{\text{SS}}$. Shorting a loop node to $V_{\text{DD}}$ after sawing was not part of the specification and was impossible since wires of the node $V_{\text{DD}}$ were nowhere near the loop.
**Figure 13.3.** Loop connected, W\_CUT is low = chip is on wafer. (Node voltage (V) vs time (\(\mu\)s).) red=W\_CUT, green=LOOPA, blue=LOOPB.

**Figure 13.4.** Loop opened, W\_CUT is high = chip has been sawn. (Node voltage (V) vs time (\(\mu\)s).) red=W\_CUT, green=LOOPA, blue=LOOPB.
Figure 13.5. Loop broken but LOOPA shorted to $V_{SS}$, $W_{CUT}$ is high = chip has been sawn. (Node voltage (V) vs time ($\mu$s).) red=$W_{CUT}$, green=LOOPA, blue=LOOPB.

Figure 13.6. Loop broken but LOOPB shorted to $V_{SS}$, $W_{CUT}$ is high = chip has been sawn. (Node voltage (V) vs time ($\mu$s).) red=$W_{CUT}$, green=LOOPA, blue=LOOPB.
Figure 13.7. Loop broken but LOOPA and LOOPB shorted to $V_{SS}$. $W_{CUT}$ is high = chip has been sawn. (Node voltage (V) vs time ($\mu$s).) red=$W_{CUT}$, green=LOOPA, blue=LOOPB.

Figure 13.6 shows the circuit behaviour with the scribe lane loop broken but node LOOPB shorted to $V_{SS}$.

Figure 13.7 shows the circuit behaviour with the scribe lane loop broken but both nodes LOOPA and LOOPB shorted to $V_{SS}$.

### 13.5 Summary

The circuit operated correctly during wafer probing and the testing of sawn die of both the fabricated TAGSYS C310 and C320 HF chips, which had their analogue circuits designed by the author for an EM Marin 0.5 $\mu$m process. The circuit allowed for a chip test mode where circuitry operates at a faster rate than normal in order to reduce wafer test time. In practice it is rare for the loop nodes to be shorted to $V_{SS}$ after sawing, but by allowing for this case a robust design was achieved.
Chapter 14

Conclusion

This chapter contains a summary of the work described in this thesis and restates the author’s contributions to knowledge. Some further work that could be undertaken by others is identified.
14.1 Introduction

This chapter summarises the work of the thesis and restates the author’s contributions to knowledge. The chapter is sectioned according to the three main themes of the work: antennas, waves, and circuits. The chapter concludes with a discussion of possible further work.

14.2 Antennas

UHF planar tags

Planar tags, or inlays, are those which have a single layer of conductor on a supporting substrate for an antenna. The tags are often glued on to products or are embedded into sticky labels which may be printed on as they are dispensed, or have preprinted logos on them to advertise a product or retailer. The type of antenna chosen for development was the thin-wire dipole in a planar form.

The reason for this was twofold.

1. Firstly for tags which are printed on-demand, a clear flat region of the tag must be provided so that the printing may be performed without interruptions by chips or antenna conductors.

2. Secondly, increasingly tag antennas are not etched from a continuous sheet of conductor but have the conductor applied by other means such as metal-vapour deposition.

Most tags have a long dimension of no more than 100 mm, which for 850 to 950 MHz operation is less than one half wavelength, but it is common for tags to be no more than 50 mm for product labels such as clothing labels. An electrically short thin-wire antenna is not particularly broadband, but by using an open-style C-shaped antenna with the tuning techniques developed by the author it has been shown that a tag can be designed with a broad enough operating bandwidth for worldwide use. The broadband tag antenna may also be used at a fixed frequency on a wide range of surfaces such as varying thicknesses of cardboard or plastic.

The author has also identified features of the C-shaped tag antenna which allow these tags to be stacked in close proximity which is suitable for retail clothing, books, and even office files.
A simulation environment was developed against well-known and trusted analysis of a half-wave dipole in order to verify that the simulator was reporting realistic results. The simulation parameters developed allowed fast simulation times with accurate results. After a validation of well-known results for simple structures, more detailed antennas were developed with confidence that they would perform as expected, as was indeed the case from empirical testing of the designed antennas.

**A two-part UHF antenna**

A two-part antenna was developed, again for a number of reasons.

1. A first part comprising a small loop antenna containing the RFID chip makes it inexpensive to manufacture.

2. By using a small loop, the testing during manufacture of the high-cost part containing the chip may be performed using a localised magnetic field avoiding stray reading which occurs when trying to confine an electric field.

3. By being in two parts, the second larger dipole antenna part may be supplied by the customer. Paper or plastic parts may have the second antenna printed directly on to the product at the time of that product’s manufacture. Paper packaging for example often includes a printing process in its own manufacture, so by adding one more colour to the printer in the form of a conductive ink, the cost of making a product RFID ready is significantly reduced.

4. Competing technologies for do-it-yourself tagging such as the manufacture of sticky labels, involves small straps containing the RFID chip which must be tightly aligned to the main antenna and attached using conductive glue. A small loop provided on a roll has been shown to require less alignment precision to the main antenna and does not require conductive glue (sometimes no glue at all in a sandwich type tag which has a sticky paper back and a glossy front). This equates to faster application of the RFID part to a label, and time is money in manufacturing. The conductive glues apart from their initial expense, cannot be stored for long times and may cure in the dispensing equipment during product changeover.
5. Tested inventories of the small loop can be on standby, and new applications or customers can be quickly supplied with labels by tailoring a secondary antenna to suit new requirements, avoiding lengthy product testing and qualification of a new tag.

The two-part tag may also allow for the RFID part to be easily peeled away from an item containing the second antenna, rendering the tag useless as required by privacy concerns. Alternatively, the second antenna may be peeled away with a small low-range tag remaining for return or warranty processing.

Again for stacking of clothing, books or files, the two-part tag was found to have extremely good performance when in close proximity to neighbouring tags. The initially separate loop part of the tag allowed an extra degree of freedom in the design of the second main antenna in order to balance inductive and capacitive coupling between close proximity tags resulting in a tag which suffered minimal detuning even when spaced 1 to 5 mm from others.

**A combined UHF and HF antenna**

Retailers are used to using HF EAS tags. Increasingly more functionality is being demanded from product labels for return or warranty, so retailers are implementing RFID and with the push of UHF EPC Gen 2 as a de facto RFID standard they are using UHF tags. Rather than have the retailer purchase a second tag and try to find room for it on their products’ labels, with a combined UHF and EAS tag in the form factor they are used to, retailers may gain the benefits of RFID but keep their EAS infrastructure in place. Their existing HF EAS systems are more resilient against false triggering than systems which attempt to read a UHF tag for theft detection, and also do not suffer from shielding effects on UHF tags from a would-be thief.

The significant contribution in designing this tag was to share as much of the structure of a typical EAS tag with the added UHF antenna. Trying to squeeze a UHF antenna along with an HF antenna on to a fixed sized small tag has in competing solutions compromised one or the other of the antennas. The author identified features of the HF tag which could be used as a UHF antenna, resulting in only a small reduction of the HF loop’s size, and a UHF antenna which was not influenced by the presence of an HF loop taking up most of the available area.
**DVD or CD tag**

The author developed a tag which could be either retrofitted on to existing discs or could be integrated into the disc itself using only the process steps already required for the manufacture of a disc other than the attachment of an RFID chip. The retrofitted version was trialled by an EPC Global industrial group which included retailers such as Best Buy and Walmart. A mock-up of a store shelf with 480 discs in normal packaging was successfully trialled by the retailers themselves. Such a validation contrasts with a carefully orchestrated demonstration by an RFID expert. The tag design was accepted as an Australian Innovation Patent.

**Integrated antenna matching network**

The matching network developed in this chapter sets out a procedure for making small loops larger than they would be if they were just a simple wire loop resonated by the RFID chip capacitance, thereby increasing the loop’s read range. The method allows a matching network to be integrated into a loop antenna, without the need for any discrete components, since to keep tag manufacturing costs low a tag should comprise only an antenna and an RFID chip.

**14.3 Waves**

**Increasing the UHF field near metal**

Tagging of metal items is always a challenge. Patch antennas are one solution but low-profile patch antennas are not very efficient and are more expensive to manufacture not only in material costs but in handling. A common substrate such as FR4 is quite lossy at UHF and more exotic high frequency materials are, at least in the author’s experience, deemed “not possible”, because of their expense.

With the advancement of “stealth” surface coatings, chemical companies have developed interesting absorbing materials. We can thank the market for mobile phones and the ever increasing use of wireless products, as use of these absorbing materials to shield internal circuits have brought the cost of these absorbers down. While still considered an expensive material, it was worthwhile exploring their use in RFID.
Sometimes RFID applications arise where the customer has a high-value product and can afford more than a few cents for a tag. Such an application was for the management of archive film lending. A 100 mm × 8 mm piece of 2 mm thick absorbing material was used under a short dipole glued to a metal canister used for archive film storage. The tag was found to work acceptably well.

Analysis of the material and some original measurement methods developed by the author showed that by using a material only 2 mm thick, 78 % of the electric field remained at that distance from the metal surface, up from the 8 % which occurs at a similar distance without the material.

A drill string identification tag

Chapter 8 details the investigation of an HF solution to tag drill strings used in oil mining. The use of ferrite and wound coils is usually avoided but this was an application where the item to be tagged is of high value. Identification allows the drill strings to be rotated in their positions in the oil well, much like rotating the tyres of a car, so that high-wearing parts may be used in a low-wear region of the well next time the drill string is inserted into the oil well.

Initially empirical testing was performed on relatively simple geometries, for example rectangular rather than circular cross section wells in metal. The performance of these simple geometries was verified by simulation. This gave confidence in the simulations so that structures which are more amenable to manufacture could be employed.

14.4 Circuits

Current reference

A low-current reference commonly used in analogue electronics was found to have two drawbacks for use in RFID: a tendency to oscillate with parasitic capacitance associated with a required resistive component; and a tendency to not start in a short time as required by a fast-moving tag or a pulsed RF system. Solutions to both these issues were developed and the circuit has been used in five commercial RFID chips.
Random-number oscillator

Simple implementations of random-number generators require two oscillators; one stable and high in frequency, and a second unstable and lower in frequency and used to gate the higher one into a counter. The output of the counter is then used as a number chosen from a maximum which is dependent upon the number of flip-flops strung together as a counter.

The carrier of an HF RFID system is quite stable as it is required to comply with EMC regulations. By developing and using a low-power divide-by-2 circuit, a stable 6.78 MHz clock was produced.

After some early failures, a slower unstable oscillator was developed. If the standard deviation of the unstable period is greater than that of the reference period, given the state of the current bit, the next bit has an almost 0.5 probability of being either a 1 or a 0. The circuit developed achieved this criterion and in RF testing chose different numbers from a maximum with a near uniform distribution.

The circuit was used in two commercial chips to randomly select a reply slot from a maximum number of slots for a chip using a slotted ALOHA anti-collision protocol.

HF rectifiers

As silicon feature sizes became smaller, the parasitic components associated with rectifier circuits, as previously designed by others, required careful attention. The chapter outlines a design evolution as processes shrank from 2 µm to 0.5 µm feature size. The change between 0.8 µm and 0.5 µm digital processes involved using different diffusion layers, such as heavily doped for the sources and lightly doped for the drains, used in forming a transistor, along with considerable reduction in oxide thickness which meant paying closer attention to node voltages, to avoid breakdown. The teaching of the chapter also includes the fact that translating a schematic into an integrated circuit requires careful identification of parasitics, and also that although feature sizes continue to shrink and have shrunk during the course of this work, the guard structures developed by the author along with the final rectifier described do minimise carriers injected into the substrate when the chip is subject to high excitation.

The rectifiers described have been used in four commercial chips.
**A passive shunt regulator**

Intellectual property developed by others on RF limiting before rectification led to the development of DC shunt regulators after the rectifier. The work covers the development of shunt regulators that, like rectifiers, evolved as process feature size and oxide breakdown voltages lowered. The circuits developed allowed for fast regulation for strong pulsed fields, but had some hysteresis so that shallow AM modulation could be detected as small dips in chip supply voltage even under conditions of strong excitation.

The circuits developed were used in four commercial chips.

**A zero-power on-wafer detector**

The time to test an RFID chip at manufacture is comparable to the cost of the chip itself. By placing the chip into a test mode the functionality of the chip circuitry can be verified in a shorter time than that required to use the RFID protocol the chip complies with in normal operation. A way to do this is speed up the internal clock of the chip while it is on the wafer and slow it back down to normal when it is a chip on an antenna. The problem is how does the chip know whether it is on a wafer or an isolated chip. The chip could contain a command detector and some circuitry at some expense in silicon area, but the chip would need to be commanded into test mode before testing commences, thus taking time. A structure can be placed into the scribe lane which separates the individual chips on the wafer, and that structure gets destroyed when the wafer is sawn.

The term low-power means two different things to an RFID manufacturer and a silicon foundry. Silicon foundries like to use their own “standard cells” since they have been verified in their customers’ designs but their customers may not have been RFID companies. Suggestions to use some combination of pull-up and pull-down resistors, some of which are destroyed and some of which are ever-present as part of the chip circuitry was suggested by a foundry. An additional issue is that after sawing, “wires” leading in and out of the scribe lane may short to the substrate or substrate-connected metal seal ring which surrounds a chip. This may cause a parasitic current path loading the chip’s supply in normal operation. In order to prevent too much parasitic current in the event that some wires are shorted, a large value resistor of some megohms may be used, but this comes at the expense of chip area. Therefore a zero-power on-wafer detector was developed.
The on-wafer detector comprised a metal link running in and out of the scribe lane and would give the correct status with any combination of shorting after sawing. The circuit was accepted as an Australian Innovation Patent and was used in one commercial chip.

14.5 Validation

The antennas and circuits developed during the course of this work were all verified by fabrication and many of them used in commercial products.

14.6 Possible further work

Possible further work that could be undertaken in the areas considered in this thesis is listed below.

- The effects of smaller feature sizes than those considered in Chapters 9, 10, and 11 could be investigated.
- The effects of more absorbing materials, as they become available, could be studied.
- The development of antennas for even closer stacking than considered in Section 2.7 might be undertaken.
- Theoretical analysis which considers coupling between multiple antennas in greater numbers might be performed.
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