A Fully Integrable Hybrid Power Management Unit for Passive UHF RFID

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***Abstract*—This paper presents a fully integrable hybrid power management unit (HPMU) realized in the 130 nm generic CMOS (complementary metal-oxide-semiconductor) process from GlobalFoundries to increase the performance of RFID tags—especially those with passively powered sensors—by intelligently managing harvested power. The HPMU strategically takes advantage of the excess harvested power beyond the operational requirements of a tag and stores this energy externally. Through intelligent power routing, this stored energy is used to sustain the supply voltage of tag circuitry during brownouts, cold starts, and for reading ranges where harvested power is inadequate to power tag logic circuits but the tag distance to an interrogating antenna is close enough to expect a backscattered response to be received by an RFID reader. This approach can reduce cold start-up time, mitigate consequences of brownouts and, effectively, extend the operational range and the responsiveness of tags—especially those with passively powered sensors. In addition, the HPMU switches off when the harvested power, indicative of a weak interrogating signal, is too low to conserve stored power. The entire HPMU has been optimized for low power consumption, which not only reduces the power overhead that HPMU introduces but also ensures that as much power as possible is siphoned and stored rather than dissipated in the power management circuitry. In off state, the HPMU consumes only around 10 nA from the external storage element and during charge storage mode of operation, the HPMU has a peak conversion efficiency of approximately 65%.**

I. Introduction

Traditionally, in the context of a fully passive (batteryless) RFID tag, the excess power above that required for tag circuity operation is not utilized. As the input power increases—for instance when the distance between an RFID tag and an interrogating antenna is reducing—the output rectified DC (direct current) increases. However, the role of a linear regulator at the rectified output is to ensure a consistent supply voltage level for tag digital logic circuitry and the tag does not benefit from occurrences of higher rectified DC output. The ability to exploit such excess energy harvested is especially significant where sensors are increasingly interfaced with passive RFID technology to realize the benefits of batteryless sensing in a range of applications in healthcare to structural heath monitoring [1]–[6].

Another problem facing applications built on purely passive RFID tags is unintentional brownouts where the power level at the output of the rectifier can drop significantly within a short period of time due to, for example, unpredictable field nulls and possible misalignment between the tag antenna and the reader antenna [7], [8]. In addition, cold start-up—time to respond to an interrogation signal by a powered down RFID tag—is typically longer with fully passive tags and consequently reduce the overall responsiveness of tags, especially those tags with integrated sensors [9]–[11].

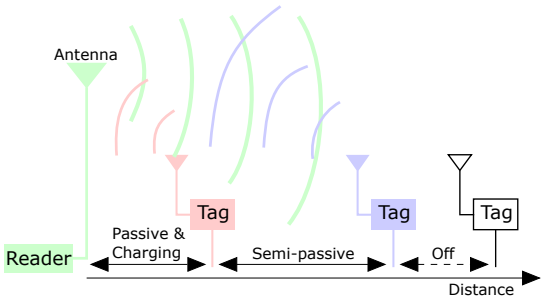

Fig. 1. Modes of operation of the hybrid power management concept.

In [8], a new concept was proposed to take advantage of excess harvested power and address the problem of brownout whilst also reducing the cold start time of a sensor enabled passive RFID tag. The operational principle is illustrated in Figure 1. Specifically, when the tag is close to an interrogating antenna, harvested power is used to power the tag circuitry and charge an external energy storage device such as a super capacitor, *ie* passive and charging mode of operation. When the harvested power drops below the operating conditions of the tag circuitry, external storage is routed to power the tag, *ie* semi-passive mode of operation. If the RF (radio frequency) field strength detected at the tag is too low and suggestive of a backscattered response not being successfully received and decoded by an RFID reader, the tag is turned off to preserve the energy in the external energy storage device, *ie* off mode.

In this paper, we build upon the proof of concept in [8]. In particular:

- We design a fully integrable hybrid power management unit (HPMU) for intelligently utilizing harvested power. The HPMU strategically routes excess harvested power to an external power storage element while maintaining adequate power to execute tag functions and routes power

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available from the external storage source when harvested power is inadequate to execute tag functions. When the incident RF field sensed by the HPMU is determined to be inadequate to successfully backscatter a tag response, power from the external storage is switched off.

- We realize the fully integrable hybrid power management unit using GlobalFoundaries 130 nm generic process and conduct simulation based experiments in Cadence Virtuoso Simulation Environment to demonstrate the functional behavior of the HPMU and evaluate the power consumption of the power management unit as well as its power conversion efficiency (PCE). We show that an optimal PCE of approximately 65% can be achieved with only a negligible power overhead provided by the HPMU.

The remaining sections of the paper are organized as follows: Section II describes the overall design of the HPMU; Section III and section IV discuss the design of the two critical functional blocks within the HPMU: the excess energy management unit (EEMU); and the power routing unit (PRU), respectively. Section V presents the simulation based experimental results of the proposed design; Section VI discusses related work and Section VII concludes the paper.

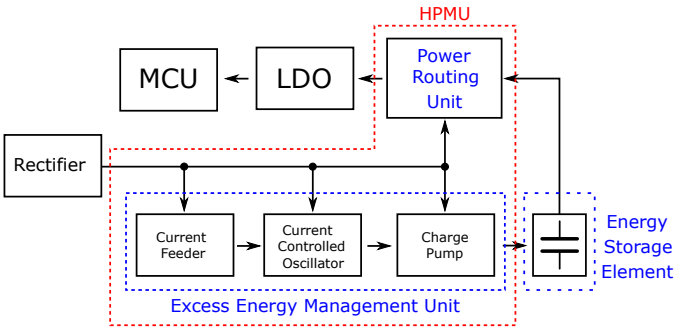


Fig. 2. An overview of the proposed hybrid power management unit (HPMU)

II. HPMU Design Overview

An high-level illustration of the proposed HPMU including the central functional blocks are depicted in Figure 2. First, the rectifier provides a DC voltage at its output. A current feeder (CF) controls the amount of current the current controlled oscillator (CCO) and the charge pump pulls from the output of the rectifier to regulate the rectifier's output at a voltage desired by the LDO (low dropout linear regulator). The current-controlled oscillator drives the charge pump to store charge in the external energy storage element. On the other hand, the power routing unit (PRU) routes either the rectified power or the stored power in the energy storage element to the LDO to power the load; in the illustration a microcontroller (MCU) such as that used in the Wireless Identification and Sensing Platform (WISP) [9].

The power routing decisions depends on the voltage level at the output of the rectifier, as we exploit the rectified DC voltage to sense the incident RF field strength, and the output of the energy storage element. Specifically, when the rectifier

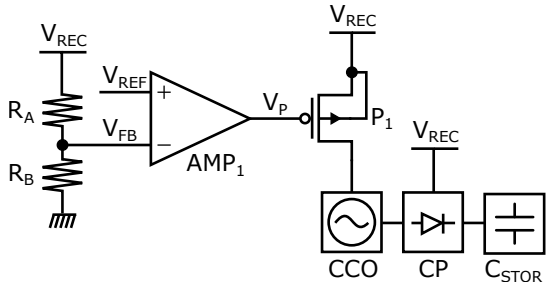


Fig. 3. The excess energy storage unit together with a super capacitor C_{STOR} as an energy storage element.

output is 2.5 V or above the rectified power is routed to power the LDO, when the rectified power is below 2.5 V the stored power is routed to power the LDO to prevent sudden power loss or brownout events. The 2.5 V limit is chosen for the design in this article because this voltage provides enough headroom for the operation of a typical off-the-shelf LDO and MCU. When the rectifier's output falls below 1 V, the system switches off as such a low voltage indicates that the tag is sufficiently far away from an interrogating antenna to successfully receive a tag response. When the rectifier's output voltage rises above 1 V, the system can be booted from the power available from the external energy storage element to significantly reduce cold start-up times.

The following sections present, in detail, the two major functional blocks: i) the excess energy management unit (EEMU); and ii) the power routing unit (PRU) of the HPMU.

III. Excess Energy Management Unit

The block-level diagram of this functional block is depicted in Figure 3. The output of the amplifier AMP_1 controls V_P so that the PMOS transistor P_1 pushes current to the CCO (current controlled oscillator) which drives the charge pump. A resistive-divided version of the V_{REC}, V_{FB} is fed to the negative input of the amplifier, forming a negative feedback loop. This loop regulates V_{REC} to be 2.5 V, when input power increases, the excess power increases and V_{REC} tends to rise, subsequently V_{FB} becomes larger than V_{REF} and the amplifier AMP_1 decreases V_P to pull more current from the V_{REC}, preventing V_{REC} from rising. On the other hand, when input power decreases, V_{REC} tends to drop, V_{FB} falls below V_{REF}, AMP_1 increases V_P to reduce the current pulled from V_{REC}, resisting V_{REC} from reducing. The amount of current available to the CCO determines its oscillation frequency, which in turns determines the energy stored in the external storage element per unit time—such as the super capacitor C_{STOR} in Figure 3. In other words, the more excess power there is, the more power will be pumped into the external storage element. In order to reduce power consumption and save chip area, the resistive ladder (*ie* R_A and R_B in Figure 3) is realized using a string of diode-connected PMOS transistors.

The design of current controlled oscillator is depicted in Figure 4. To achieve a low power design, the CCO consists of a current starved inverter, a Schmitt trigger and an inverter to

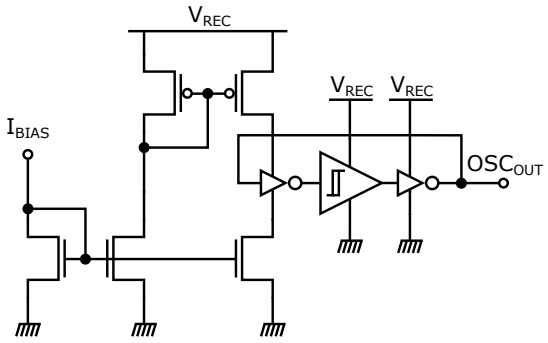


Fig. 4. The low power current controlled oscillator (CCO).

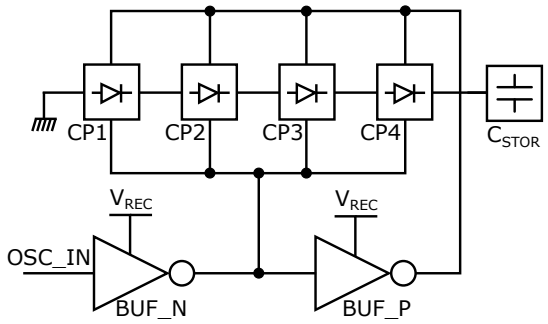


Fig. 5. The four stage charge pump (CP).

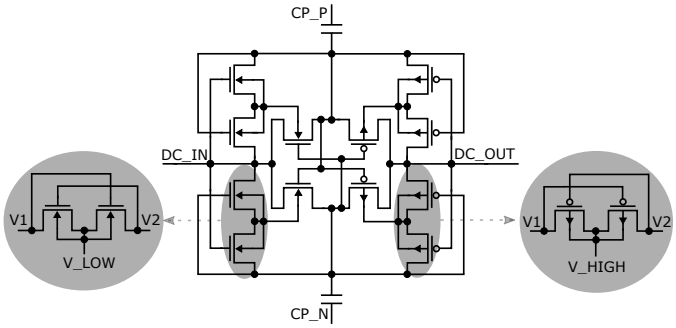


Fig. 6. A single differential drive rectifier stage with dynamic bulk biasing used for the first three charge pump stages—CP1 to CP3—illustrated in Figure 5.

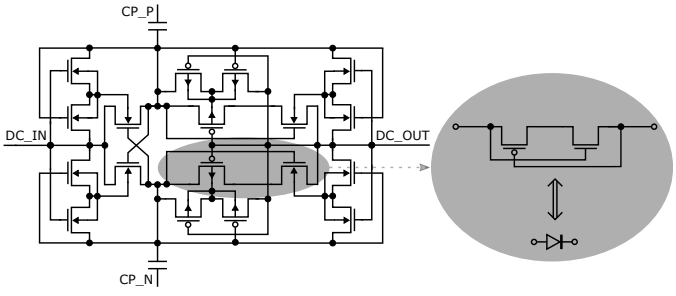


Fig. 7. The last charge pump stage—CP4—implemented with complementary CMOS diodes to prevent reverse leakage.

provide the additional phase shift. The CCO output is fed to two inverters which provide enough current capability to drive the charge pump, as shown in Figure 5.

The charge pump, shown in Figure 5, employs a cross-coupled differential-drive structure which achieves higher efficiency than the classical Dickson charge pump [12]. Due to the relatively high differential input, parasitic diodes of transistors can be easily turned on and degrade efficiency and stability. Thus, as shown in Figure 6, two auxiliary PMOS transistors are used to bias the bulk of every PMOS transistor in the main rectification chain to the higher of the input AC or the output DC. Similarly, two auxiliary NMOS transistors are used to bias the bulk of every NMOS transistor in the main rectification chain to the lower of the input AC or the input DC voltage. As such, the bulk terminal of all transistors are biased such that no parasitic diodes can be turned on. The last stage of the charge pump, as shown in Figure 7 exploits complementary CMOS diodes [13] to prevent reverse leakage and loss of charge already stored in an energy storage element. Similar to the previous stages, the PMOS and NMOS pairs are exploited in the last stage—CP4 in Figure 5 and Figure 7—for appropriate bulk biasing. It is also worthing mentioning that the voltage level of the storage element is clamped at around 4 V to avoid over-charging. The 5 V tolerant LDMOS (Laterally-diffused MOS) devices in the process are employed for circuits that need to operate at high voltages.

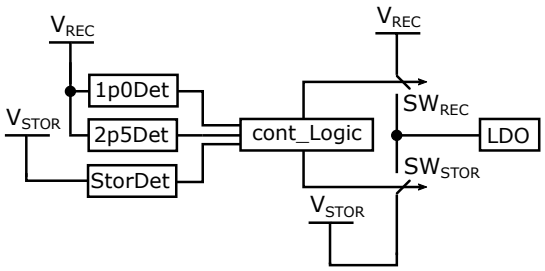
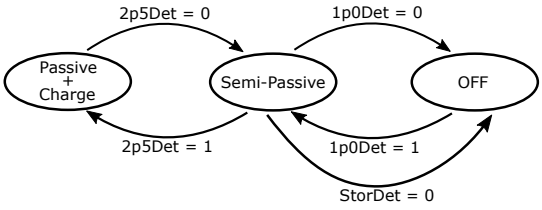


Fig. 8. Power routing unit (PRU).

IV. Power Routing Unit

As shown in Figure 8, the power routing unit consists of a 1 V voltage detector (**1p0Det**) and a 2.5 V voltage detector (**2p5Det**) for the rectified DC output voltage and an energy storage element voltage detector (**StorDet**) which asserts output at 3.6 V and de-asserts its output at 2.5 V. The output of three voltage detectors are fed into the control logic to determine the control signals to the two switches $\mathrm{SW_{REC}}$ and $\mathrm{SW_{STOR}}$ to realize the active power routing as discussed in Section I. The control sequence of the logic circuitry is depicted in Figure 9.

For these three voltage level detection circuits, both the 1 V detection and energy storage element voltage level detection are designed to operate with very little power in all modes of operation highlighted in Figure 9. However, the 2.5 V detection for the rectifier is designed to operate with low power in semi-passive mode and OFF mode and operate with



	SW_{REC}	SW_{STOR}
Passive + Charge	ON	OFF
Semi-Passive	OFF	ON
OFF	OFF	OFF

Fig. 9. Control logic of the power routing unit for the operating modes illustrated in Figure 1.

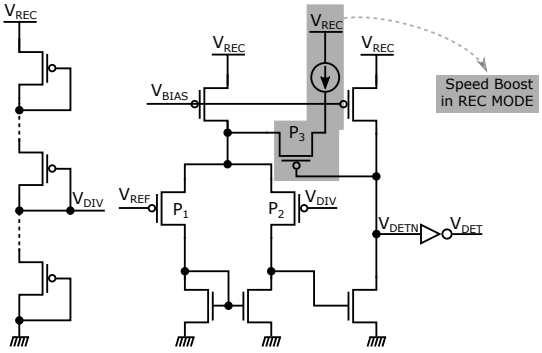


Fig. 10. 2.5 Volt threshold detection circuit with a response speed boost in Passive and Charging mode.

moderate power in the passive and charging mode to improve the speed of detecting the rectified output falling below 2.5 V, such as in a brownout event, and re-routing power from a storage element to maintain the responsiveness of a tag. Detailed implementation of this voltage level detection circuits is shown in Figure 10. In Figure 10, when $\mathrm{V_{REC}}$ rises above 2.5 V, its divided version $\mathrm{V_{DIV}}$ exceeds $\mathrm{V_{REF}}$, $\mathrm{V_{DETN}}$ is pulled to ground and the PMOS switch $\mathrm{P_3}$ is closed, thus additional current is pushed into PMOS differential pair ($\mathrm{P_1}$ and $\mathrm{P_2}$) to improve speed. In contrast, when the rectifier's output voltage falls below 2.5 V, the bias current into the differential pair is reduced, thus reducing the power consumption.

The design of the power routing circuitry requires solving two key challenges: i) the design of control logic circuits requiring voltage translation to translate logic levels based on two different and varying supply voltages; and ii) the design of power switches.

A resistively loaded common source stage shown in Figure 11 is used as the voltage level translation structure. When $\mathrm{V_{IN}}$ is low the resistor at the drain of the transistor pulls the node $\mathrm{V_{OUTN}}$ to be the supply voltage to be translated to, then the inverter pulls $\mathrm{V_{OUT}}$ to ground. On the other hand, when

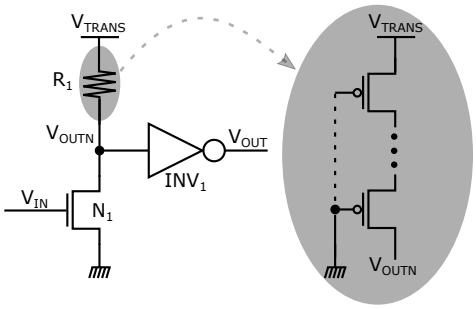


Fig. 11. The voltage level translation circuit.

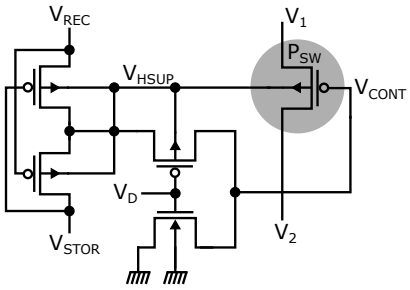


Fig. 12. The smart PMOS switch designed to ensure the the control voltage $\mathrm{V_{CONT}}$ is selected from the higher of the two supply voltages—$\mathrm{V_{REC}}$ and $\mathrm{V_{STOR}}$.

$\mathrm{V_{IN}}$ is high, the NMOS transistor $\mathrm{N_1}$ is turned on to pull the node $\mathrm{V_{OUTN}}$ to ground, then the inverter pulls $\mathrm{V_{OUT}}$ to the supply voltage to be translated to. This structure allows us to translate between the two supplies (*ie* $\mathrm{V_{REC}}$ and $\mathrm{V_{STOR}}$) that are not only different but also varying. The voltage translation is needed to ensure for the proper operation of the control logic under all conditions. It is worth noting that the resistor $\mathrm{R_1}$ is realized using stacked PMOS transistors.

Our design for the power switch is shown in Figure 12. It is designed to ensure when the gate of the PMOS switch $\mathrm{P_{SW}}$ is pulled high, the control signal $\mathrm{V_{CONT}}$ of the PMOS switch comes from the higher of the two supply voltages—in our case $\mathrm{V_{REC}}$ and $\mathrm{V_{STOR}}$. PMOS is used for the design of the power switches to achieve a lower on state resistance during conduction. The PMOS pair shown in Figure 6, is employed to select the higher voltage of $\mathrm{V_{REC}}$ and $\mathrm{V_{STOR}}$. When $\mathrm{V_D}$ is high, the gate of the PMOS switch is pulled to ground through the conduction of the NMOS transistor, thus the switch is closed. When $\mathrm{V_D}$ is low, the gate of the PMOS switch is pulled to the higher voltage of $\mathrm{V_{REC}}$ and $\mathrm{V_{STOR}}$, thus the switch is opened.

When the power switch is in *on* state, the gate of the PMOS is pulled to ground to conduct current. When it is in *off* state, the gate of the PMOS should be pulled high so that it exhibits very high resistance. However, as a consequence of the two varying supply voltages, we can enter a situation where the source terminal of the PMOS, being connected to the other supply domain, is at a higher voltage potential than the supply voltage that the PMOS switch is controlled by; such a possibility can effectively leaving the switch in a partially *on*

state. However, our smart switch circuit shown in Figure 12 is designed to ensure when the gate of the PMOS switch is pulled high, the high signal is emanating from the higher of the two supply voltages——in our case V_{REC} and V_{STOR}.

V. Simulation Results

The complete HPMU is realized in the GlobalFoundaries 130 nm generic process and simulation based experiments are conducted in Cadence Virtuoso Simulation Environment. We investigate three aspects related to the HPMU: i) power conversion efficiency in the passive and charging mode of operation to understand the amount of excess power that can be directed to a storage element; ii) the power consumption of the HPMU in the various modes of operation; and iii) the transient behavior of the HPMU under different operating conditions to verify the active power management capability of the HPMU.

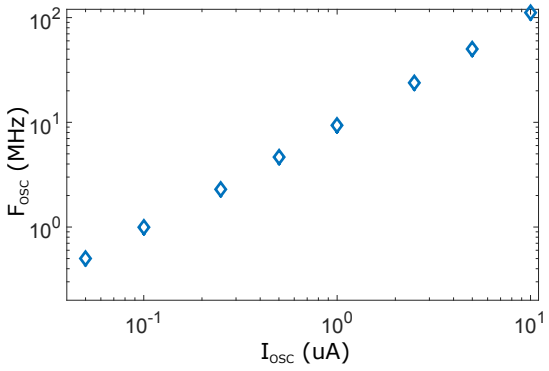


Fig. 13. The output frequency of the CCO as a function of the current consumed.

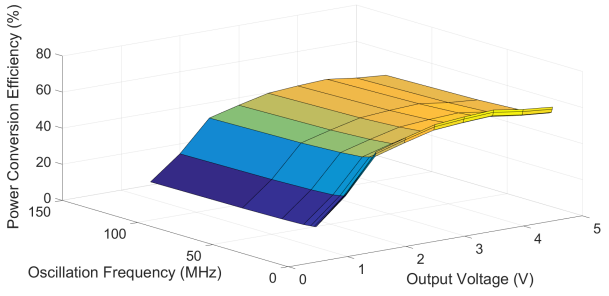


Fig. 14. The relationship between the power conversion efficiency (PCE) of the charge pump (CP), oscillator frequency and the output voltage of the charge pump.

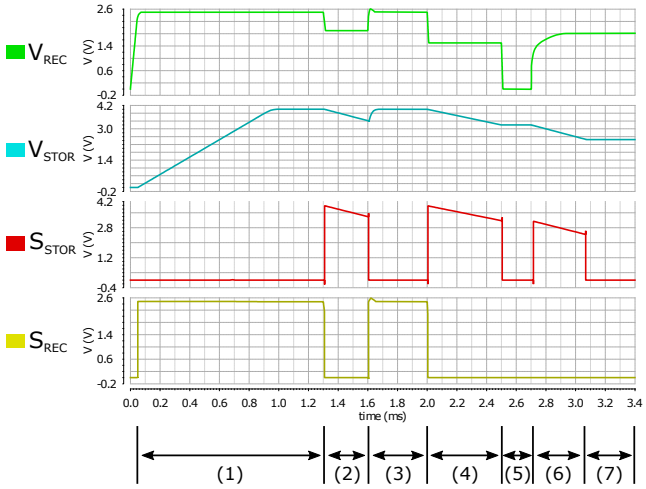
The oscillator frequency and current consumption of the current controlled oscillator, and the power conversion efficiency (PCE), are depicted in Figure 13 and Figure 14, respectively. It can be observed in Figure 14 that the optimal PCE (65 %) can be achieved around an output voltage of 2.5 V to 3.5 V, which is the voltage range that the charge pump will be operating predominately at during the passive and charging mode of operation. It can also be observed that the PCE does not significantly degrade over the range of operational frequency.

The power consumption of the HPMU is summarized in Table I. It is worth noting that the CF, CCO and CP do not operate in the semi-passive and OFF mode. In the passive and charging mode, their power consumption can vary and depends on the excess harvested power. Thus, it is more meaningful to express their power conversion efficiency rather than the absolute power consumption as shown in Figure 14. The control logic in the PRU consumes negligible static current, thus after the system enters a state, its power consumption is negligible. When the rectifier's output is 2.5 V, the available current at the rectifier's output V_{REC} is in the order of 100 uA, hence our HPMU poses less than 2% power overhead.

TABLE I
Power Consumption Summary

Modules	Passive & Charging	Semi-Passive	OFF
CF	Variable	N/A	N/A
CCO	Variable	N/A	N/A
CP	Variable	N/A	N/A
1p0Det	10 nA	10 nA	10 nA
2p5Det	2 uA	10 nA	10 nA
StorDet	10 nA	10 nA	10 nA

The simulation transient of the HPMU is shown in Figure 15. Here, V_{REC} and V_{STOR} are DC voltage levels of the rectifier's output and the external storage element, and S_{REC} and S_{STOR} indicates whether the rectified power or the power stored in the capacitor is supplying the LDO regulator. The varying V_{REC} is emulated by changing the power level at the input of the rectifier. In addition, in this simulation experiment, the external storage element is modeled by a 10 nF capacitor to achieve shorter simulation time.



(1) Passive + Charging	(4) Semi-passive	(7) OFF
(2) Semi-passive	(5) OFF	
(3) Passive + Charging	(6) Semi-passive	

Fig. 15. System-level simulation to verify behaviour of the HPMU.

To demonstrate that the reduced cold start-up time can be achieved with HPMU, the start-up time required for the system

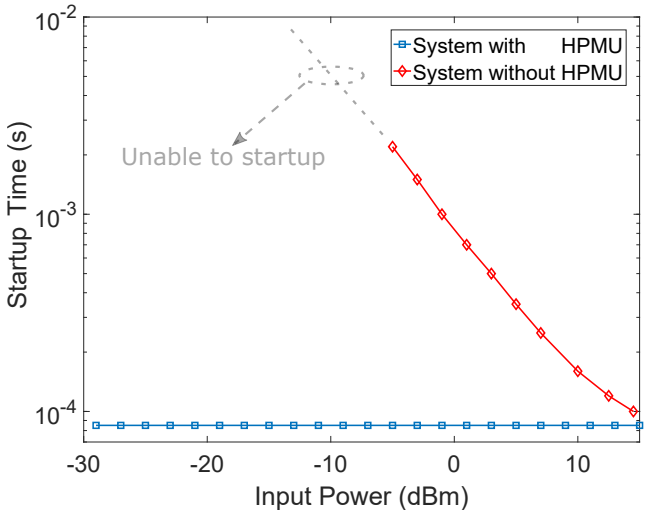


Fig. 16. Cold start-up times for systems with and without HPMU at different input power levels.

with and without HPMU at different input power levels are plotted in Figure 16. It can be observed in Figure 16 that when the input power is very high (e.g. 13 dBm), the start-up time required for both systems are approximately the same. As the input power decreases, the startup time required for the system without HPMU increases because the energy needed has to be harvested and accumulated over time, thus it is highly dependent on the RF field strength. On the other hand, the HPMU routes power directly from the external energy storage element, thus start-up time is significantly shorter and does not depend on the input power level. As discussed previously, systems without HPMU requires V_{REC} of 2.5 V for start-up whereas systems with HPMU only requires 1 V, corresponding to input power levels of -5 dBm and -29 dBm respectively. Hence, HPMU dramatically improves input power sensitivity of the overall system.

VI. Related Works

Achieving reliable operation of passive devices, including sensor enabled RFID tags, exploited other approaches such as the integration of alternative ambient sources of power such as solar power to accompany the harvested RF power to realize hybrid powering scheme [14], [15] or the use of multi-band power harvesters [16]. Such approaches also provide an effective approach to the problems we have considered with the added requirement of integrating additional mechanism on passive devices such as solar panels, relatively large wideband antennas and additional hardware including multiple rectifiers and power summations stages to capture ambient power.

Charge burst schemes are another well-established approach to harvest power [17]–[19] and they typically involve collecting charge over time in the "charge phase" and subsequent use of this energy to supply the system in a significantly shorter "burst phase", to potentially extend operational range. However, performance and responsiveness of applications built on such approaches are sacrificed due to the long "charge phase" are still subjected to the indeterministic nature of RF power harvesters as highlighted in [14]–[16].

A related design for power routing is offered in the enerchip CC from Cymbet [20] and was employed in [8] to realize the proof of concept hybrid power management unit. However, enerchip CC makes its power routing decisions in response to only one threshold voltage level. More importantly, the key differences that sets this work apart from enerchip CC are: i) we attempt to convert all of the excess energy by pulling as much current as necessary from rectifier's output while regulating this voltage at a defined threshold; and ii) enerchip CC consumes significantly higher amounts of power to realize its power routing functions.

To the best of our knowledge, there are no existing integrated solutions in the literature for actively managing harvested power of passive RFID tags by storing and intelligently routing power as proposed in this study to overcome brownouts, cold-start problems and achieve a highly responsive tag platforms to support emerging applications looking to integrate not only identification but sensing capability to passive RFID tags. Further, out proposed architecture can be integrated to actively manage other ambient sources of power such as solar and customized to suit the needs of target device platforms.

VII. Conclusion and Future Work

This work presents a fully-integrable hybrid power management unit built on the proof of concept in [8]. Our design is unique in that it actively manages the harvested power to reduce brownout events, shorten cold start-up times and extend operational range as well as realize more responsive tags, especially those requiring higher power due to integrated sensors. We have demonstrated and validated the design through simulation based experiments in Cadence Virtuoso Design Environment and we showed that our design converts and stores excess power with very high efficiency and consumes negligible power compared to the available power at the rectifier's output. In the future, we will consider power harvesting together with power management and propose it as a complete power solution for passive RFID tags.

Acknowledgment

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