Design and optimisation of power rectifiers for passive RFID systems in monolithic CMOS circuit.

Behnam Jamali, Damith Ranasinghe, Peter Cole
School of Electrical and
Electronics Engineering
The University of Adelaide
S.A. 5005 AUSTRALIA
Email: {bjamali, damith, cole} @eleceng.adelaide.edu.au

ABSTRACT

In this paper, we present and analyze the most fundamental constraint of RFID systems, power rectification. This issue plays an important role in development of long-range RFID systems. Rectifiers are the key components in power rectifications and efficiency of an RFID system. Therefore this paper is concentrated in investigating this major issue. To tackle this problem a novel Schottky Barrier Diode (SBD) has been proposed. The proposed SBD provides good power conversion rate and switching properties.

Keywords: CMOS, Schottky Diode, Power rectification, Passive RFID

1. INTRODUCTION

Passive radio frequency identification (RFID) systems provide an inexpensive means to automatically and accurately capture information remotely. This facility combined with the Internet provides immediate and accessible delivery of information.

A goal of this project was to design a new transponder tag with increased reading range and reliability which is able to handle anti-collision algorithm by using a new voltage rectifier/multiplier topology by employing a very well matured standard CMOS process. The technology used is a four-metal, two-poly $0.35\mu m$ digital CMOS process supporting E^2PROM. Advanced low-voltage, low-power circuit design techniques and fast control logic circuits have been employed.

A passive RFID tag draws power from the RF field created by an RFID reader and uses it to energize its circuitry. It does this by rectification of the reader's radiated RF field using rectifying circuitry. The power then available to the tag is dependent upon both the available field strength and the efficiency of the rectification process. One option for increasing the operating range of an RFID system without increasing the reader's field strength is to increase the efficiency of the tag's rectification structure. A major component of any rectification circuit is a diode type device and so, the first part of this project was focused on the design and implementation of a novel high efficiency Schottky Barrier Diode (SBD) on a standard CMOS process. The forward voltage drop of the SBD diode was investigated and analytic equations formulated considering the Schottky barrier drift region resistance and the contributions from the p^+ guard-grid. A design procedure to minimize the drift region resistance for any blocking voltage was derived. The fundamental trade-off between the forward voltage and leakage current in the novel SBD concept was determined

Based on the critical review of the Schottky diodes fabricated in the first part, new structures of novel SBD were designed to address most of the open issues related to its reverse break-down voltage and series resistance. Detailed analysis of the important design parameters of the novel Schottky barrier diode were performed using HSPICE with the parameter set used in the calibration process. The novel structure was also compared to an alternative fabrication approache, specifically, a NMOS and PMOS gate-cross-connected bridge. The comparison

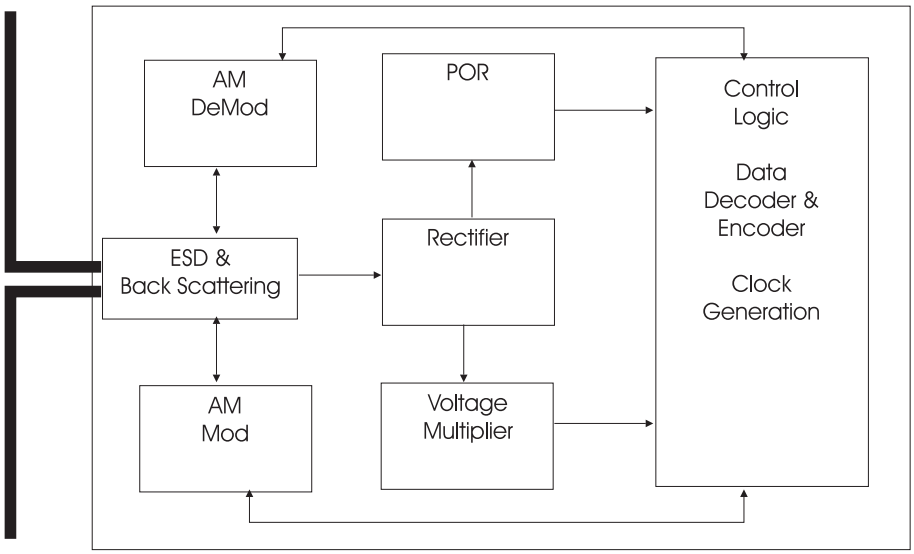


Figure 1. Architecture of a transponder RFID IC.

shows that the novel structure provides higher figure of merit for power rectification.

In the later part of the project, an analysis of circuit advantages enabled by the novel SBD were performed. The circuit simulation showed that by utilizing the novel SBD the operating frequency of the circuit can be increased to the UHF region while maintaining approximately the same power efficiency as that achievable when using a discrete Schottky diode. This leads to the possibility of dramatic improvements in size, weight and cost of the RFID transponder circuits.

Passive RFID systems increase productivity and efficiency in every segment of the global supply chain. RFID labeling has a number of advantages over conventional bar code systems. The optics based bar code system could be rendered useless due to common everyday environments containing dirt, dust, smoke, grease, condensation, disorientation and misalignment. Furthermore bar codes are subject to fraudulent duplication and counterfeiting. As such the need for low cost high volume and small size transponder tags is increasing. At the same time stringent regulation of transmit power and bandwidth have to be met. In order to meet this requirement it is necessary to build a very low power transponder.

Clever techniques exist to build Schottky diodes but they are fabricated with special processes which are not available in a full-scale standard CMOS fabrication facility. The purpose of this paper is to describe a layout design which can be used to implement Schottky diodes in standard normal CMOS process. That means that the design can be directly implemented into a standard CMOS process without adding costly procedure steps or Mask layers.

This paper presents a design procedure and fabrication of a Schottky Barrier Diode (SBD) diode in commercially standard $0.35\mu m$ CMOS technology. The specially designed Schottky Barrier Diodes with low series resistance allow high frequency conversion of the received RF input power into dc supply voltage.

In order to reduce the series resistance of the Schottky contact, interdigitating the fingers of the Schottky diode layout was adopted. This technique increase the perimeter of the contact while keeping its area to minimum, so in effect, not only does it decrease the junction capacitance but also it reduces the series resistance. Interdigitating

also greatly reduces the distance from anode to cathode, mitigating the likelihood of electrons being swept down to the substrate.

Sections *II* and *III* describe the system architecture and the Schottky diode properties and design layouts.

2. ARCHITECTURE

Figure 1 shows a block diagram of a transponder IC. In the following paragraph we will cover each of the individual block diagrams in more detail. The most important section of a transponder IC is its power supply. The power supply consists of a voltage multiplier that converts a part of incoming RF signal power into dc voltage to power up all the active circuit elements on the chip. A 300pF reserviour capacitor stores and filters the supplied energy.

2.1. DC Supply Voltage Generation

The dc power is generated form the incident RF signal by a voltage rectifier/multiplier as shown in Figure 2. The diodes used in the voltage rectification are Silicon-Titanium Schottky diodes with low series resistance and low junction capacitance.

2.2. Voltage Multiplier

The high voltage during erase and programming of the *EEPROM* are generated by an on-chip charge pump. It is responsible to convert the dc voltage of about 2 volts to a voltage of approximately 14 volts needed for programming eeprom circuit. The charge pump utilizes the same Schottky diodes as the one of the power supply.

2.3. Power On Reset

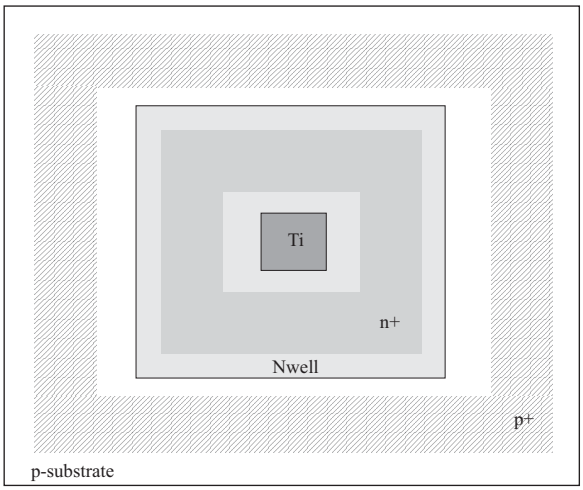
Power on Reset circuit provides voltage supervisory circuit to monitor power supplies in the transponder. It asserts a reset signal whenever the V_{cc} supply voltage falls below a reset threshold. Reset remains asserted for an interval after V_{cc} has risen above the threshold voltage.

2.4. Modulator and Demodulator

A reader talks to a tag using AM modulation in its forward link. Therefore an AM demodulator (an envelop detector) is used in transponder to shift the carrier frequency of an amplitude modulated signal to a lower frequency and to recover the signal sent by the reader.

A tag talks to its reader using Amplitude or Phase modulation. As such an appropriate modulator is required to modulate and back-scatter the incident signal. When the downlink is active, the reader transmits a continues wave carrier with some small gaps for the tag to syncronise its response.

3. DESIGN AND LAYOUT OF SBD



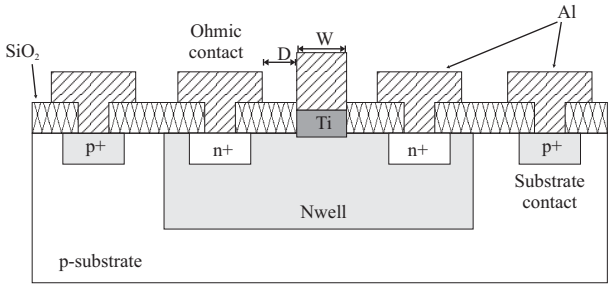


Figure 2. Cross sectional view of a planer Schottky Barrier Diode.

3.1. Theory and Background

In designing a Schottky diode for RFID systems, both non-linearity of the capacitance and the RC cutoff frequency of the diode are of primary concern. A brief discussion of the diode fabrication is necessary at the outest because the parasitics of the diode are a function of its geometry and physical implementation. Implementing diodes on a standard CMOS process is designed specifically for ease of integration into circuits where the devices must be heavily packed and fabricated as a monolithic system. Figure 2 shows a cross-sectional view of the Schottky Barrier diode that was fabricated for this project. It consists of a Schottky contact to an n-well active region and ohmic contacts to a heavily doped n+ layer. With this diode geometry the layout is compact and the extrinsic parasitics are minimized. That is an important factor for high frequency operation of the circuit.

Figure 3 shows a cross-sectional view and the schematic of the Schottky diode and its associated equivalent circuit elements. The Schottky contact has width of W, the length of the diode into the plane of the page is L and the separation between Schottky contact and ohmic contact is D. The capacitance of the Schottky diode, $C = \epsilon WL/d$, which is from the depleted space charge region with depth, d, where d is a function of applied reverse bias and is given by:

$$d = \sqrt{\frac{2\epsilon kT}{q^2 N_d} V_{bias}} \tag{1}$$

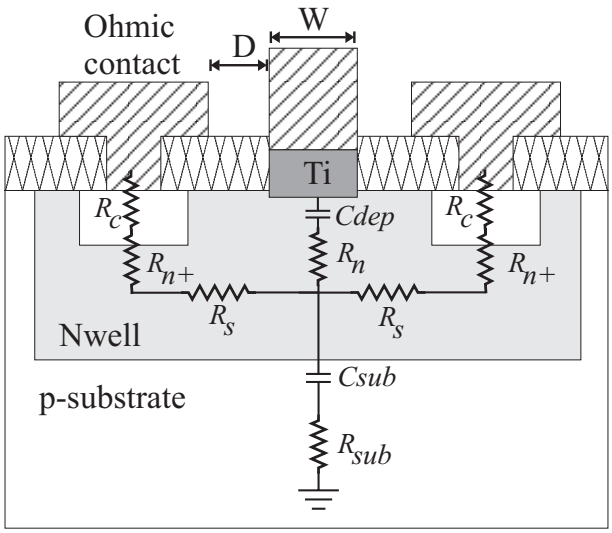


Figure 3. Equivalent circuit of Schottky diode, illistrating the various components of the series resistance.

The sum resistance in series with this capacitance, R_{sum}, can be modeled as the sum of four components. The first element, R_n, is the n-well vertical resistance through the un-depleted portion of the n-well layer, where, the amount of un-depleted material is a function of bias. A $0V$ bias is used as a conservative value because this resistance will be at its largest value, that is given by:

$$R_n = \frac{1}{WL} \cdot \rho_n \cdot T_{undep} \tag{2}$$

where ρ_n is the resistivity of the n-well material and T_{undep} is the thickness of the undepeleted region at $0V$ bias. Because this is a sheet resistance, it is an area term and so its value is inversly proportional to $W \cdot L$. The second component of the resistance is the spreading resistance, R_s, that acccounts for the spreading of the current flow under and around the Schottky contact into the n-well region. Value of R_s is given by:

$$R_s = \frac{1}{3} \cdot \frac{W}{4} \cdot \frac{1}{L} \cdot \frac{\rho_n}{T_n} \tag{3}$$

where ρ_n is the resistivity of the n-well material and T_n is thickness of the n-well layer. A factor of $W/4$ comes form the fact that the current travel only half the contact width as it spreads out to either side and that these reistances are in parallel. Another additional factor of $1/3$ arises form the distributed nature of the spreading resistance and capacitance under the contact, which is analoges to the spreading resistance in the base of a bipolar junction transistor or distributed resistance of the gate finger of a MESFET.

The third component, R_N, comes from the resistance of the N+ contact region due to the separation between the n-well and ohmic contacts:

$$R_N = \frac{1}{2} \cdot \frac{D}{L} \cdot \frac{\rho_{N+}}{T_{N+}} \tag{4}$$

and again the factor of $1/2$ arises because there are two in parallel. The final component of the series resistance, R_c, is from the ohmic contacts:

$$R_c = \frac{1}{2L} \sqrt{\rho_{cont} \cdot \frac{\rho_{N+}}{T_{N+}}} \tag{5}$$

where ρ_{cont} is the specific contact resistivity. Because R_s, R_N, and R_c are inversely proportional to L and the capacitance is directly proportional to $W \cdot L$, decreasing W and increasing L to maintain a constant diode area reduces R_{sum} in proportion to C and consequently increases f_{cls}, which is defined using the large signal capacitance of the diode:

$$f_{cls} = \frac{1}{2}\pi C_{ls} R_s \tag{6}$$

This is analogous to the design of the base-emitter junction of a bipolar transistor where the dominant resistance is the base resistance, which is also a periphery dependent term, so by decreasing the emitter stripe width, the $R_{base}C_{eb}$ time constant is reduced.

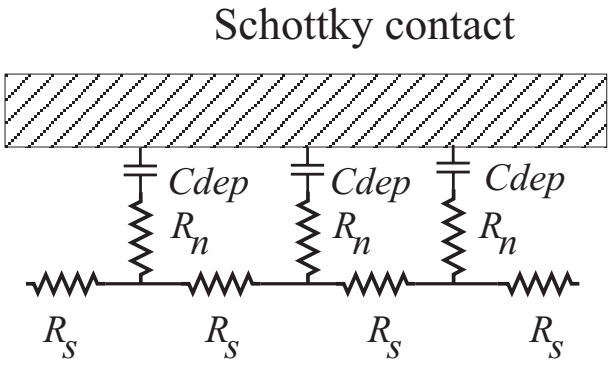


Figure 4. Diagram, illistrating the distribution nature of the resistance and capacitance of the Schottky contact.

Equation 6 for the diode cutoff frequency is valid at low frequencies, but neglects several high frequency phenomenon that adversely affect the series resistance of the diode. The following discussion of these effects is taken directly from the work by Champlin and Eisenstein[4] and also includes their references to original work. Dickens[5] was the first to treat this problem in the context of a Schottky diode and showed that the high-frequency extension of the spreading resistance is an impedance Z that for circular geometries given by:

$$Z = \frac{1}{2\pi\sigma a} arctan(b/a) + \frac{(1+j)}{2\pi\sigma\delta} \ln(b/a) \tag{7}$$

where b and a are the radii of the semiconductor and contact, respectively, σ is the dc conductivity of the semiconductor and δ is the skin depth given by:

$$\delta = \sqrt{\frac{2}{w\mu_0\sigma}} \tag{8}$$

in which μ_0 is the magnetic permeability.

Equation 7 is based on two assumptions that are not generally valid for semiconductors in the sub-millimeter wave region. They are

$$w \ll w_{dr} = \frac{\sigma}{\epsilon} \tag{9}$$

where w_{dr} is the dielectric realisation frequency and

$$w \ll w_{scat} = \frac{q}{m^* \mu_e} \tag{10}$$

where w_{scat} is the scattering frequency, m_e^* is the effective mass of the electrons and μ_e is the mobility of the electrons. Making assumption 9 is tantamount to ignoring the displacement current and is the usual assumption that leads to 8. Assumption 10 is equivalent to ignoring the inertial mass behavior of the carriers in their response to an applied electric field.[6]

Both assumptions can be removed from 7 by replacing the dc conductivity σ with the complex quantity

$$\sigma^{'} + jw\epsilon = \sigma\{\frac{1}{1 + j(w/w_{scat})} + j(w/w_d)\} \tag{11}$$

and by replacing $(1 + j)/\sigma$ with the actual propagation constant of the semiconductor material:

$$\begin{aligned} \gamma &= \sqrt{jw\mu_0}\sqrt{\sigma' + jw\epsilon} \\ &= \frac{(1+j)}{\delta}\{\frac{1}{1 + j(w/w_{scat})} + j(w/w_d)\}^{1/2} \end{aligned} \tag{12}$$

Substituting 11 and 12 into 7 and assuming $(b/a) \gg 1$ leads to $Z = Z_s + Z_0$ where Z_s is the complex bulk-spreading impedance given by:

$$Z_s = \frac{1}{4\sigma a}\{\frac{1}{1 + j(w/w_{scat})} + j(w/w_d)\}^{-1} \tag{13}$$

and Z_0 is the complex skin-effect impedance. With a buried N_+ layer doped as heavily as possible, $N_D \approx 5 \times 10^{18} cm^{-3}$ and $\rho_{N+} = 7.5\ \Omega \cdot \mu m$, the skin depth at 1 THz is $1.4\mu m$. Since the layer is only $1.0\mu m$ thick, the current crowding effect will be negligible in the frequency range of interest, and Z_0 can be neglected.

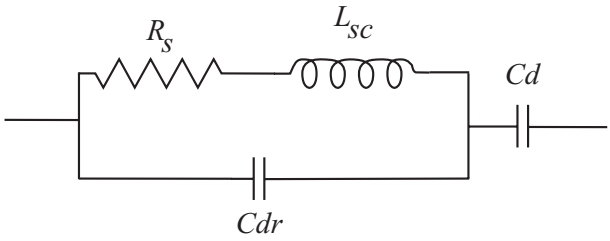


Figure 5. Equivalent circuit model of a Schottky diode that includes the effects of the displacement capacitance.

An equivalent circuit model including Z_s is shown in Figure 5 These high frequency effects can be modeled by adding two elements to the equivalent circuit model: a displacement capacitance $C_{dis} = 1/R_s w_{dr}$ and an inertial inductance $L_{scat} = R_s/w_{scat}$ The parallel $L_{scat}C_{dis}$ circuit is resonant at the plasma frequency given by:

$$w_{pl} = 2\pi f_{pl} = \frac{1}{sqrtC_{dis}L_{scat}} = \sqrt{w_{dr}w_{scat}} \tag{14}$$

For the diodes used in this work, the n-well active region was doped at a level of $N_D = 1.0 \times 10^{17} cm^{-3}$, for which $f_p = 3.0THz$. Because the operating frequencies of the circuits are well below these, the use of the simple RC model to calculate f_{cls} as a figure of merit is valid.

Other factors, though, limit how far W can be effectively reduced. As W approaches dimensions similar to the n-well layer thickness, the lateral extent of the depletion region around the edges becomes significant, and effectively increases the area of the diode, a problem that has been solved analytically by others.[7] The real

problem is that as the depletion depth increases under reverse bias, the lateral depletion region becomes proportionately larger, flattening out the C-V curve. This effect can be eliminated by using a self-aligned guard-ring to remove the n-well layer not directly under the Schottky contact, so there is no material remaining to become laterally depleted.

3.2. Models and Parameters of the SBD

Numerical device modeling and simulation are essential for analyzing and developing semiconductor devices. They help a design engineer, not only to gain an increased understanding of the device operation, but also they provide the ability to predict electrical characteristics, behavior and parameter effects that influence the device behaviour. With this knowledge and abilities the designer can design a better structure, estimate the device performance, perform worst case analysis and optimize device parameters to yield an optimized device performance.

As in any device simulator, any quantative, or qualitative simulation of a device, relies heavily on the device models and their parameter values. Although many device models with their default parameters are available in many commercial simulators, some of their parameters do not provide realistic characteristics of the semiconductor materials. As for the SBD developed in this work, there is no model available that takes into account all the parameters affecting its performance.

Therefore, it is important to develop a model for the SBD fabricated on a standard CMOS process. In developing a model the following were the main purposes taken into consideration:

- To define the electrical circuit equivalent of the SBD structure to enable improved analysis of circuit performance.
- To define the magnitude and location of relevant parasitic electric elements to enable prediction of performance effects.
- To manipulate parasitic elements to obtain improved or enhanced circuit performance.
- It shall consist of conventional lumped circuit elements.
- It should accurately re-produce the diode IV characteristics and S parameters.
- It shall be compatible with the commonly used simulation tools.

The aim of this section is to analyze the applicability of CMOS material parameters from the literature and measurements, and implement them into SPICE program as a way to calibrate the simulation process with the real device characteristics.

3.3. Simplified Model

Figure 6 shows a simplified model developed for the Schottky diode fabricated on a standard CMOS process. Data collected with measurement tools in the later phase of this work, was used to develop and refine this model. The refining process was done through iterative data collection and analysis and comparing expected results with actual data.

In this figure L_i and L_o are the anode and cathode series wire inductance respectively. C_i and C_o are the input and output capacitance. C_f is the equivalent capacitance of the interdigitating fingers of anode and cathode. R_i and R_o are the anode and cathode parasitic n-well resistance to the substrate (or Gnd). D_{pn} models the parasitic n-well to p-substrate pn junction diode. Its characteristics can be obtained from the Spice model file supplied by the foundry. R_2 is the n-well vertical resistance just above the D_{pn} diode.

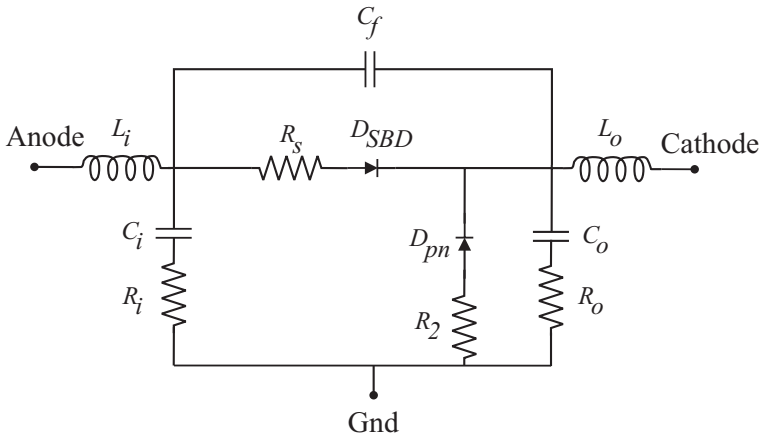


Figure 6. Equivalent circuit model of a Schottky Diode.

4. FABRICATION AND MEASUREMENT

A brief discussion of the diode fabrication is warranted at the outset because the parasitics of the diode are a function of its geometry and physical implementation. This novel Schottky diode is designed specifically for ease of integration into circuits where the device must be densely packed. As such this section concentrates on the fabrication process, its limitations and the ways to get around those limitations.

Despite the popularity and economic advantage of CMOS the lossy nature of its substrate has made the implementation of analog circuits at high frequency is difficult. As operation frequency increase the undesirable parasitic effects of silicon substrate becomes more and more dominant. The purpose of this paper is to describe layout design improvement for Schottky diode fabrication on a standard CMOS process. In the first fabrication two types of Schottky diodes were implemented, p-type and n-type.

P-doped Schottky diodes are good for application requiring very low turn on voltage. But they exhibit a low break-down voltage and high series resistance. Therefore they are not suited for RFID application. Also, as the work function (electron affinity) of Titanium is very close to that of the p-substrate, a Schottky diode cannot be formed by using the aforementioned technique. The result of using such a method is an ohmic contact to p-substrate area. Therefore the only type of Schottky diode that can be implemented in standard CMOS process is the n-type one.

As in a standard CMOS process, we have no control over doping concentration and the type of the material used, the only parameter that can be controlled is the size of the junction. In order to get a high efficiency rectifier, it is essential to have Schottky diodes with high saturation current I_s, which results in low forward voltage drop, low junction capacitance C_j, small series resistance R_s, and also low parasitic capacitance to substrate C_{sub}. A large junction Schottky diode results in a large saturation current and small series resistance, but also large junction and substrate capacitance. Those large capacitances would dominate the diode characteristics, so the optimum junction size of the diode needs to be found. For comparison, Table 1, shows the different Schottky junction sizes that were implemented.

From the discussion in the previous chapters we know that the series resistance of the n-well is relatively high. This manifests itself as the series resistance of the Schottky diode. This was compensated by interdigitating the

*The SD1 and SD2 have same junction area, but SD1 anode and cathode are connected by metal1 while the anode of SD2 is connected out by metal2. That would make the cathode contacts to surround the junction.

†Extra-long junction dimension Schottky Diode is fabricated to verify our understanding over the dimension effects.

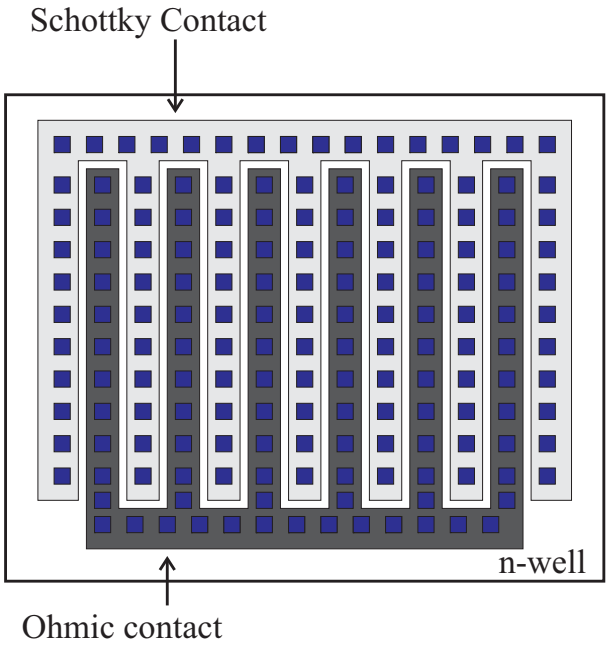


Figure 7. Top view of multi-finger Schottky contact diode.

fingers of the ohmic and Schottky contacts. The distance between the ohmic and Schottky contacts was also reduced to the minimum allowable by the CMOS design rule-set. This technique increased the perimeter of the contact while keeping its area to minimum, so in effect, not only does it decrease the junction capacitance but also it reduces the series resistance. Interdigitating also greatly reduces the distance from anode to cathode, mitigating the likelihood of electrons being swept down to the substrate. Figure 7 shows a layout view of the Schottky diode including the guard ring around it.

5. CONCLUSION

Schottky diodes provides a highperformance, cost-effective solution for today's circuit designs for RFID applications. In this paper we presented a novel passive UHF transponder power supply circuit. Theoretical analysis used for optimization of the design have been presented. The fabrication process used is a $0.35\mu m$ CMOS technology process with E^2PROM capability. With a new Schottky diode and voltage generation topology presented in this paper, careful layout design and antenna matching, a long read range can be achieved. The barrier height of the Schottky contact was measured to be about 0.45eV. The advantage of this Schottky diode is its low cost as it does not require any extra masks or steps and can be implemented monolithically in an standard CMOS process.

Table 1. Prototyped Schottky diode junction sizes

No	Area (pm^2)	Perimeter (μm)	Fingers	W × L (μm)
SD1	0.23	1.92	1	0.48 × 0.48
SD2 *	0.23	1.92	1	0.48 × 0.48
SD3	1.4976	7.20	1	0.48 × 3.12
SD4 †	16.128	72.90	6	0.48 × 5.6
SD5	14.4	60.96	1	0.48 × 0.30

REFERENCES

1. K. V. S. Rao, "An overview of backscattered radio frequency indentification system (RFID)",in Proc Asia Pacific Microwave Conf,. Vol3, Singapore: 1999.
2. B. L. Sharma, "Metal-Semiconductor Schottky Barrier Junction and their Applications" New York: Plenum 1984
3. Hudait M K "Electrical transport characteristics of Au/n-GaAs Schottky diodes on n-Ge at low temperature" Solid State electron 2001
4. K. S. Champlin and G. Eisenstein, "Cutoff frequency of submillimeter Schottky-barrier diodes," Microwave Theory and Techniques, vol. MTT-26,no. 1, pp. 31-34, January, 1978.
5. L.E. Dickens, "Spreading resistance as a function of frequency" Microwave Theory and Techniques, vol. MTT-15, no. 2, pp. 101-109, February, 1967.
6. K. S. Champlin, D.B. Armstrong and P.D. Gunderson, "Charge carrier inertia in semiconductors," Proceedings of I.R.E., vol. 52, no. 6, pp. 677-685, June, 1964.
7. B. Gelmont, M. Shur, and R.J. Mattauch, "Capacitance-voltage characteristics of microwave Schottky diodes," Microwave Theory and Techniques, vol. MTT-39, no. 5, pp. 857-862, May, 1991.