Analysis of a UHF RFID CMOS rectifier structure and input impedance characteristics

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ABSTRACT

Passive radio frequency identification (RFID) systems deployment efforts are revolutionizing supply chain logistics by providing unprecedented supply chain visibility. The widely used bandwidth of operation in modern systems is the UHF ISM (industrial, scientific, and medical) band. The performance of UHF RFID systems are largely reliant on low power CMOS circuits, efficient power rectification and the ability of RFID label antennas to match to the input impedance of the RFID label IC. This paper examines a new rectifying structure and considers it for its merits in RFID applications while analysing contribution of the rectifying structure to the input impedance of RFID chips as this is an important consideration in impedance matching to an external antenna.

Keywords: CMOS, Schottky Diode, Power rectification, Passive RFID

1. INTRODUCTION

A simple illustration of the concept of a Radio Frequency Identification (RFID) system is provided in Figure 1. Here a transmitter of interrogation signals which is contained within an interrogator communicates via electromagnetic waves with an electronically coded label to elicit from the label a reply signal containing useful data characteristic of the object to which the label is attached. The reply signal is detected by a receiver in the interrogator and made available to a control system.

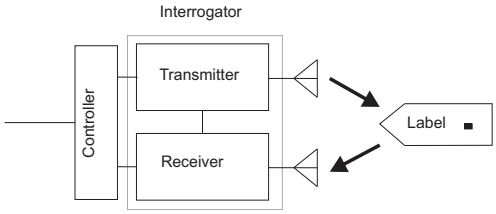

Figure 1: Illustration of an RFID system.

There is a wide range of operating principles for such a system [1,3]. The operating principle and operating frequency are driven principally by the application of the labelling system and the constraints provided by electromagnetic compatibility regulations, environmental noise, and the ability of fields to permeate a scanned region of space or to penetrate intervening materials. Applications are found in reliable and secure data collection, object or personal identification and authentication, and the detection of location of scanned objects [2].

In a primary category of passive systems the most common operating principle is that of RF backscatter [2] in which a powering signal or communication carrier supplies power or command signals via an HF or UHF link. However the circuits within the label operate at RF or lower, and reply via sidebands generated by modulation, whin the label, or part of the powering carrier. This approach combines the benefits of relatively good propagation of signals at HF and UHF and low power of operations of microcircuits at RF or lower. Powering at UHF is employed when a longer interrogation range (several meters) is required, and HF powering is employed when electromagnetic fields which exhibit good material penetration and sharp spatial field confinement are required or very system implementation cost is desired.

In the category of active labels the most common objective is to obtain a long range. Some active labels are battery-assisted backscatter labels while other types of active labels may not use backscatter but instead use a battery for

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powering and transmitting requirements (independent reply generating labels). This paper examines and presents practicable solutions to extending the lifetime of such active labels by using turn-on circuits to prolong the lifetime of the battery and hence the lifetime of the label. The lifetime of a label is also an important consideration in the use of high performance long lifetime theft detection labels.

2. A UHF RFID CHIP

A label antenna, that in the context of RFID applications is preferably inductive, and the rectifying circuit that is intended to produce a rectifying voltage used for powering the label circuits, can be modelled as indicated in Figure 2. Here R_r represents the antenna radiation resistance, X_s represents the antenna reactance, X_l represents the reactance of the diode capacitance, X_B is the reactance of the reservoir capacitor that also serves as an RF bypass, R_l represents the loss in bringing reactive power into and out of the diode junction capacitance, and R_a is the ohmic loss contribution from the antenna.

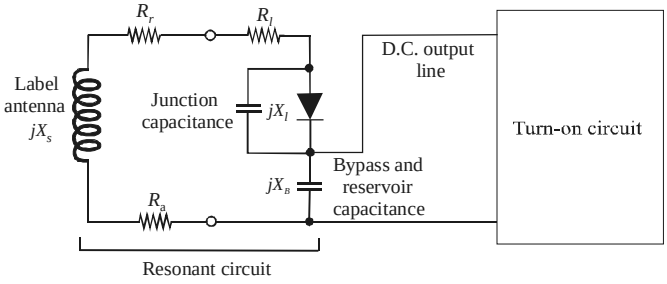

Figure 2: A simple overview of a label rectification circuit

The antenna ohmic losses can be ignored since the antenna construction in a good design can be a slot antenna containing a significant amount of copper. In addition the series combination of the impedance jX_l and jX_B will be approximately equivalent to that provided by the diode junction capacitance, as the reservoir capacitor has a relatively larger capacitance of the order of 100 pF. It is assumed that no d.c. power is removed from the diode. By shaping the antenna and its connection points appropriately, an impedance match between R_r and R_l can be achieved.

3. POWER RECTIFICATION

The DC power supply voltage is generated from the incident RF signal power by the means of a voltage rectifier in contactless passive RFID technology. At HF ISM band, 13.56 MHz, it is more common to use diode connected transistors or a MOSFET bridge rectifier. The most common structure of the bridge rectifier consists of two nMOS and two pMOS FETs [4]. The output voltage of such a circuit, however, suffers from the voltage drop across the transistors because of the MOSFETs' threshold voltage. Therefore further away from the interrogator antenna, where the RF signal is weaker, this kind of rectifier might fail to operate properly.

Therefore, there is a need for a device that can operate from a lower input voltage level. The Schottky diodes developed in this dissertation satisfy these conditions. The voltage drop of a SBD is approximately 200 mV, at 10 µA, as was confirmed by experimental work. A new organization of these diodes can be used to deliver a high voltage to the chip from the weak input RF signal.

Although voltage multiplier circuits are widely used in CMOS, the description of the kind of circuit presented in this paper has only been restricted to operating principles and a thorough and systematic treatment has not been presented. In this paper, the voltage doubler realized with SBDs is thoroughly analyzed and a complete model is proposed. Its degradation features and its implication on tag circuitry endurance are studied and experimental results supporting the proposed method are presented.

4. COMPARISON OF RECTIFIER STRUCTURES

RFID designers, traditionally use MOS bridge rectifiers, as shown in Figure 3 [4]. Although these structures are well suited for low frequency, they perform inadequately at UHF. It worth mentioning that with advancement in CMOS

circuits and availability of new submicron transistor feature sizes, it may be possible to build a UHF rectifier from MOSFETs. However, the turn-on threshold voltage of such a configuration is normally much higher (≈ 300 mV) than that of a Schottky diode rectifier structure. Plots in Figure 4 shows a comparison of a Schottky diode rectifier with a MOS bridge configuration. It is evident from the plot, the MOS bridge rectifier has a sluggish response to the input signal. The MOSFET models used for this simulation are derived from AMI submicron fabrication with feature size of 0.35 µm. A more comprehensive study of different rectifier topologies can be found in [5].

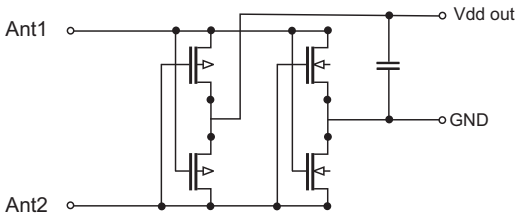

Figure 3: MOS bridge rectifier network.

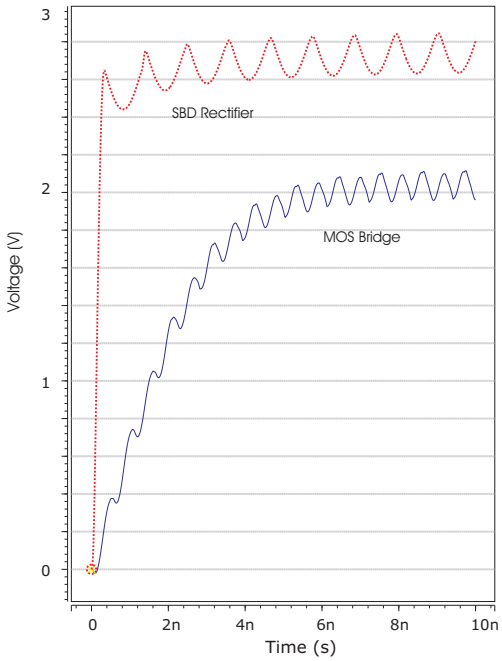

Figure 4: Comparison of the response time of a SBD diode with a MOS bridge rectifier circuit.

5. VOLTAGE DOUBLERS

A voltage doubler, also referred to as a charge-pump in the context of memory ICs, provides a voltage that is higher than the voltage of the power supply. In many applications such as EEPROMs, flash memory, filters and switched capacitor transformers a voltages higher than the power supply are frequently required. The increased voltage levels in a charge pump are the result of transferring charge to a capacitive load. Its ability to provide voltage amplification makes it suitable as rectifier structure of tags' power supplycircuitry, where the normal range of operating voltage is limited.

Charge pumps operate by switching on and off a large number of MOSFET switches which charge and discharge a large number of capacitances, transferring energy to the output load. A large amount of energy is lost whenever the load current is changed. For example, where there is no load, the circuit still operates but with 0% efficiency. Savings of switching energy can be achieved by regulating the switching frequency whenever a requirement for the load current

changes. In addition, simulation and measurement results indicated a strong dependence of the output voltage on the load resistance [6].

In practical implementations, a number of issues related to parasitic capacitances, leakage resistances and the operating frequencies have to be considered. Power loss in a charge pump must be minimized both to protect the integrated circuit from overheating and to improve the power conversion efficiency. Most of the resistive power loss results from current through the diode. Dynamic power loss occurs as a result of switching charge pump capacitors. Diodes with a large junction area have smaller series resistance, minimizing the resistive power loss. This, however, results in larger junction capacitance that increases dynamic power loss and also limits the operating frequency of the charge pump.

5.1 Current techniques in CMOS

In Figure 5(a), a charge-pump circuit that uses diodes as the charge transfer device is shown. It is based on the Dickson's design. The output voltage of a diode charge pump is given by [7]

$$V_{out} = (V_{dd} - V_t) \times N \,. \qquad 1$$

In (1) V_t is the voltage drop in the diode and N is the number of stages. The term (V_{dd} - V_t) may be called the voltage gain per unit stage and its output voltage linearly increases as the number of stage increases. Because forming independent diodes in the same substrate is very unwieldy and the voltage drop across the diode is not scalable, the conventional charge pump proposed by Dickson [8] uses the diode-connected MOSFET as the charge transfer device in place of the diode.

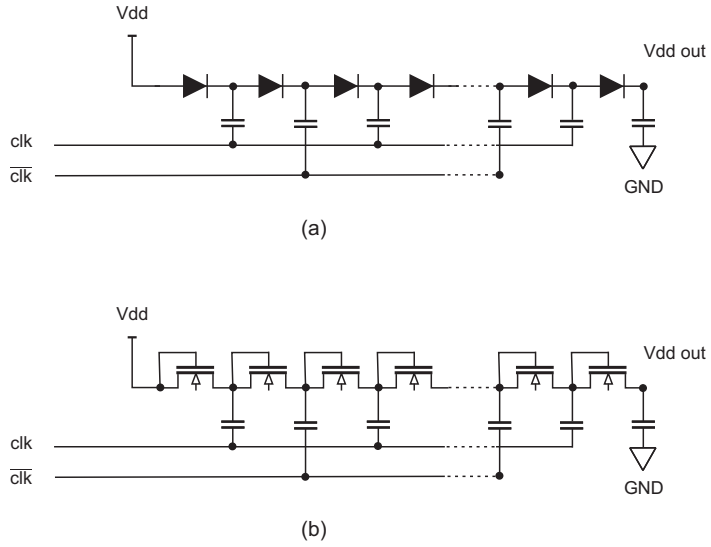

Figure 5 Functional diagram of (a) diode based Dickson charge pump and (b) a functional diagram of a traditional Dickson charge-pump.

In the Dickson charge-pump circuit as shown in Figure 5(b), as the voltage of each stage increases by the charge pumping, the threshold voltage of the diode-connected MOSFET increases due to the body effect. The voltage gain *Vdd* −*Vt* decreases and the output voltage becomes lower than the value obtained by the diode charge pump. Therefore, the output voltage of the Dickson charge pump cannot be a linear function of the number of stages and its efficiency decreases as the number of stage increases.

Several attempts have been made to alleviate the loss problem in the Dickson's design [9], but they must use a very complex timing scheme or backward control which may have a risk of reverse current even with auxiliary MOSFETs [4]. Use of floating devices [10] to eliminate body effects has also been reported, but the resulting charge-pump may generate substrate current by floating the device.

In [11] a detailed analysis of a Dickson multiplier built in VLSI technology with diodes realized by nMOS transistors is provided. They considered effects of threshold voltage and leakage current. Most of the charge pump applications require a two-phase clock. A high-efficiency charge pump can be constructed using cross-coupled voltage doublers consisting of four power nMOS, four power pMOS [12]. But all of the above require auxiliary circuits or power transistors and capacitors that occupy a large area.

6. PROPSED RECTIFICATION STRUCTURE

A bridge rectifier based on the SBD diodes cannot be used in a CMOS circuit, because when the input voltage swings to its negative value, it drives the cathode of the SBD diode into the negative region. That condition will make the n-well at lower voltage with respect to the p-substrate. In such a scenario, the parasitic diode D_{pn}, as shown in Figure 6, becomes forward biased, causing a large amount of current to flow from n-well to the substrate. This phenomena is similar in analogy to the latch-up condition of an inverter in a CMOS circuit.

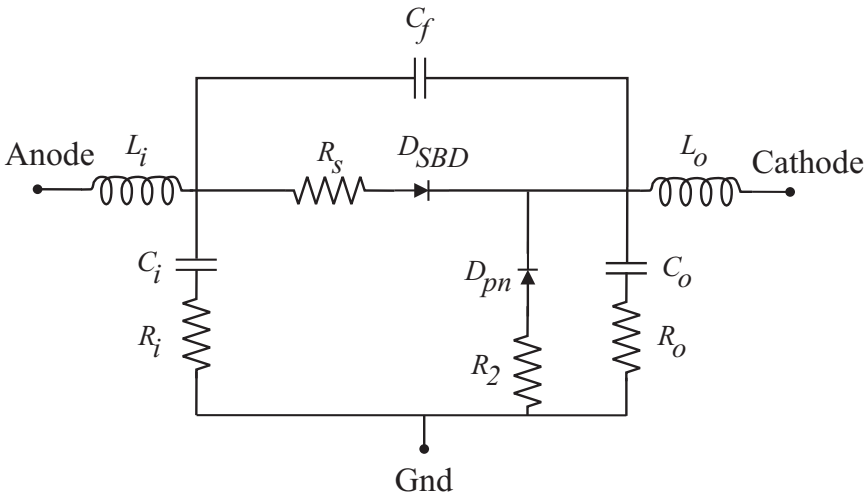

Figure 6: Equivalent circuit model of a Schottky Diode on standard CMOS process outlined in [13].

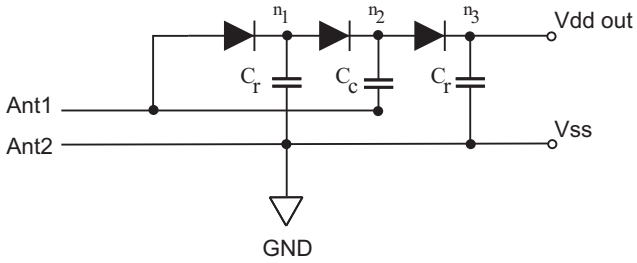

Figure 7: A novel rectifier/multiplier topology using the SBD, based on Dickson's design.

In Figure 7 a new approach based on Dickson's voltage multiplier design is proposed. In this circuit diodes are Silicon-Titanium Schottky diodes, developed in this dissertation. These SBD diodes have low series resistance of less than 500 and low Schottky junction capacitance of approximately 500 fF. The schematic shown in Figure 7 is simplified and does not show the capacitances that anode and cathode of the SBD makes to the ground or substrate. However, these capacitances are included in the diode model for simulation. For this configuration to operate the antenna needs a DC connection through it.

These diodes are connected to the antenna pins by poly-poly capacitors. From RF point of view, assuming that the *Cr* and *Cc* have low impedance, the junction capacitance of these diodes are connected in parallel. For DC, however, they are connected in series to allow a DC current to flow from V_{dd} to V_{ss}. For a short explanation of its operation assume that the *Ant2* is connected to the ground and the *Ant1* is connected to a sinusoidal voltage source of amplitude V_{in}, furthermore assume that the pump starts with all the capacitors depleted of any charge. In phase I, the voltage doubler starts by rising Ant1 from zero to $+V_{in}$. Capacitor *Cr* is charged to voltage $V_{in} - V_d$, where V_d is the voltage drop across the diode and C_c is assumed to have no charge.

In phase II, the input voltage will swing to $-V_{in}$. The voltage across *Cc* is now $V_{in} + (V_{in} - 2V_d)$. Subsequently when the pump goes back to phase I, the voltage at node n2 now rises to V_{in} plus the voltage access C_c and the charge stored by C_c is now shared with C_r at node n_3 and the final output voltage at node n_3 is equal to $2V_{in} - 3V_d$. Thus the charge sharing allows the output voltage to grow to a level higher than the input voltage. In Figure 8 a multi-stage charge pump of the above configuration is depicted. A detailed analysis can be performed to show that the voltage generated at the output of this circuit to a good approximation is given by

$$V_{dd} = (V_i - V_d) + nV_\Phi - (n+1)V_d - nV_l\,, \qquad 2$$

where V_i is the RF input signal amplitude, V_d is the voltage drop across the diode, V_Φ is the voltage swing at a node due to capacitive coupling with the input signal, V_l is the voltage drop due to the output current and *n* is the number of stages.

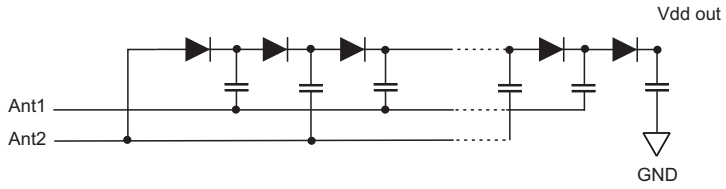

Figure 8: A multi-stage multiplier schematic based on the Schottky Barrier Diode (SBD).

In the above equation, the voltage swing, V_Φ, can be calculated in terms of the reservoir capacitor, *Cr*, coupling capacitor *Cc* and parasitic capacitor (due to interconnect wires), *Cs* as given in (3).

$$V_\Phi = V_i\left(\frac{C_r}{C_r + C_c + C_s}\right) \qquad 3$$

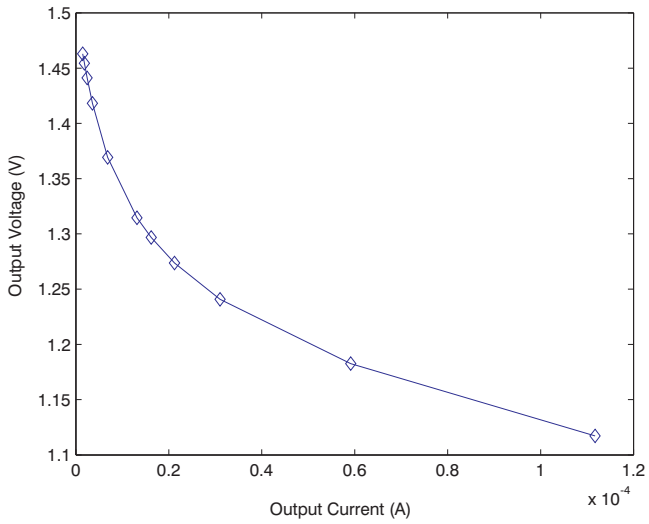

Figure 9: The output voltage as a function of the output current for a two stage charge pump.

Figure 9 shows the output voltage of a two stage charge pump as the output current is increased. As can be observed from the plot, the voltage drop, V_l, is directly proportional to output current, *Io*, and inversely proportional to operation frequency, *f* and the total node capacitances, *Cr* + *Cc* + *Cs*, therefore,

$$V_l \propto \frac{I_o}{f \cdot (C_r + C_c + C_s)}. \qquad 4$$

This is only true assuming $T << RC$, ie. the load time constant is much less than the charging time constant.

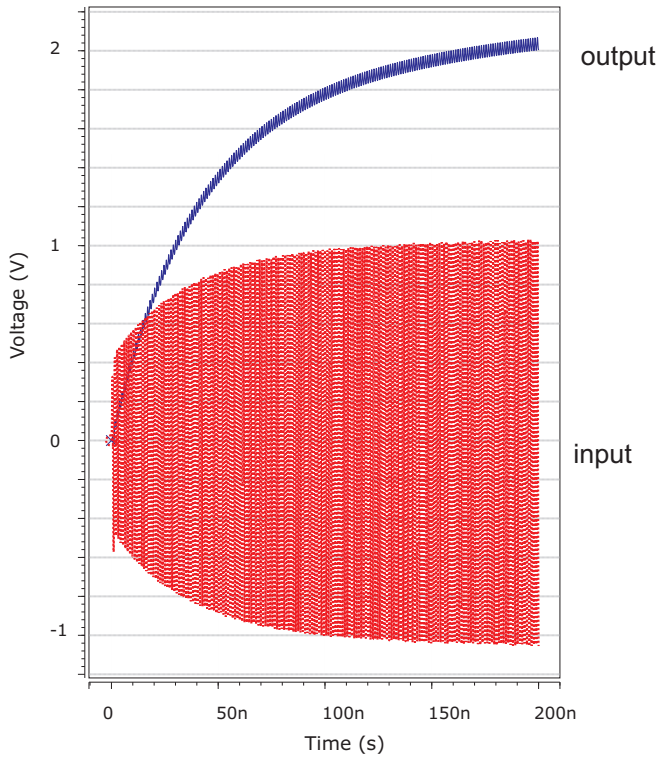

Figure 10: Plot of input and output of a single stage voltage multiplier circuit.

Figure 10 shows the input-output relation of a single stage voltage multiplier circuit. It consists of three diodes and three capacitances. As expected, the output voltage is almost twice the input. An n-stage cascade of the above design will produce almost (Vi × n) V output voltage. By choosing an appropriate number of stages, any voltage can be reached. However, this is only valid for negligible current draw. As soon as there is output current, there is also an AC current through the capacitors, resulting in a voltage drop and a lower input voltage for subsequent stages. In fact, numbers much higher than, for instance, 10 or 20, are not sensible in practice.

Plot of the empirical data shows that the output voltage drop, *Vl*, is a cubic function of the number of stages *n*. Using least-square curve fitting technique and statistical analysis, one can find the coefficients of a polynomial, *p*(*n*), of degree 3, that fits the empirical data. In the above case Matlab was used to simplify this process. Equation 4 can now be rewritten as (5) given below.

$$V_l = \frac{I_o}{f \cdot (C_r + C_c + C_s)} \left(\frac{2}{3} n^3 + \frac{1}{2} n^2 - \frac{1}{6} n \right). \qquad 5$$

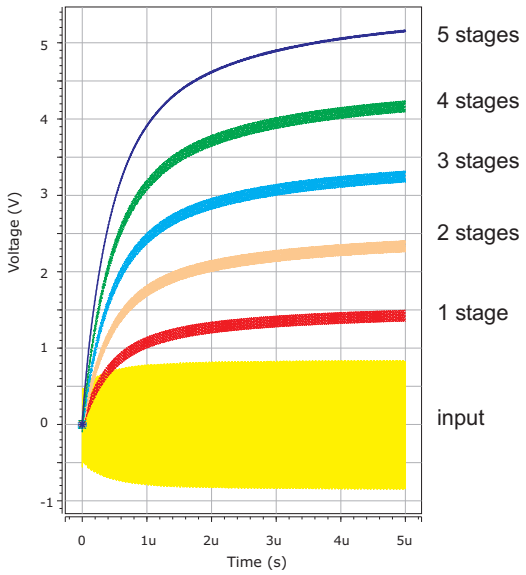

Figure 11: Comparison of output voltage versus input from 1 to 5-stage case.

7. EFFECTS OF C_C AND C_R ON OUTPUT VOLTAGE

These capacitors work as a charge transfer device. They get charged during the negative cycle of the input and transfer their charge to the output during the positive cycle of the input RF signal. Therefore a small value would decrease the time required to transfer the charge from one stage to the next. A large value on the other hand, would increase the RC time constant and would act as a low pass filter to the input signal. Thus, they cannot have an arbitrary size. Figure 12 shows the effect of these capacitors on the output voltage of the charge pump.

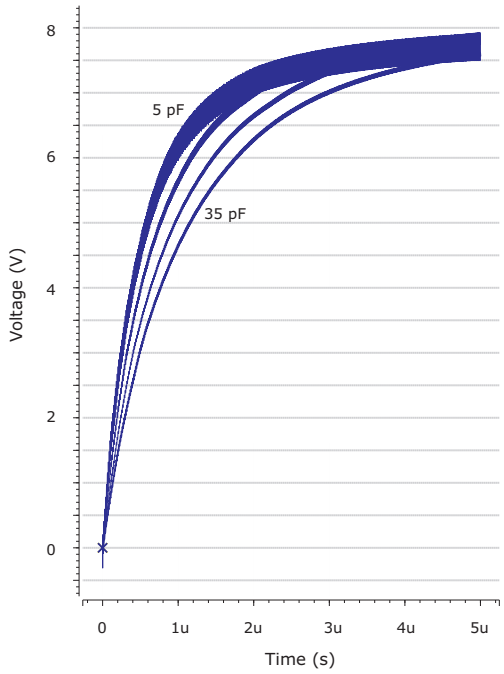

Figure 12: Effects of C_c and C_r on the output voltage.

For these capacitors, it is important to have small parasitic resistance, R_s and capacitance, C_{sub}. However C_{sub} is proportional to the desired capacitance C_c and C_s, because a capacitor value is proportional to its area. The value of C_c, C_s and C_{sub} can not be made arbitrarily small since a certain amount of coupling is needed. The best way to minimize C_{sub} is to build the capacitors (lateral capacitors) formed by multi-finger top metal layer configuration or making use of the capacitance between the top two metal layers. To minimize R_s, large aspect ratio or multi-finger capacitors can be used. Also, using top metal layer would minimize the amount of charge lost to the substrate.

The capacitors designed for this project were laid out using multi-finger configuration with the minimum distance allowed, according to the design rules, between the fingers. The value of these capacitors were chosen such that it would dominate the capacitance of the n-well to substrate, which has a value of almost 0.3 pF, acording to AMI process specifications.

8. INPUT IMPEDANCE

The effectiveness of communication between the RFID reader and a tag can be increased by maximizing the power transfer from the antenna to the rectifier structure. It can be shown mathematically that a source will deliver its maximum power to the load when the impedance of the load is a complex conjugate of the impedance of the source. This is achieved through impedance matching.

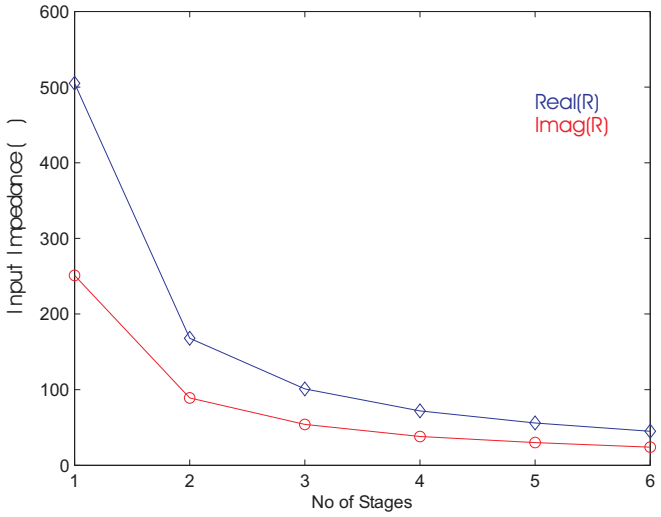

Figure 13: Plot of input impedance vs. number of stages in the rectifier structure.

The plot in Figure 13 shows the input impedance of the charge pump versus its number of stages. As it is evident from the plot, the higher the number of stages the lower the input impedance will be, therefore, in practice there is a limit to how far one can introduce more stages. As a comparison Table 1 shows the measurement results performed on two RFID chips from two different manufacturers. The Open port measurement was performed to help with the de-embedding of the results.

Table 1: Measured chip impedance values (26/05/2005).

Chip manufacturer	Input impedance Ω
Alien C1G2	24 - *j*154 Ω
TagSys 6408	15 - *j*174 Ω
Open Port	6 – *j*358 Ω

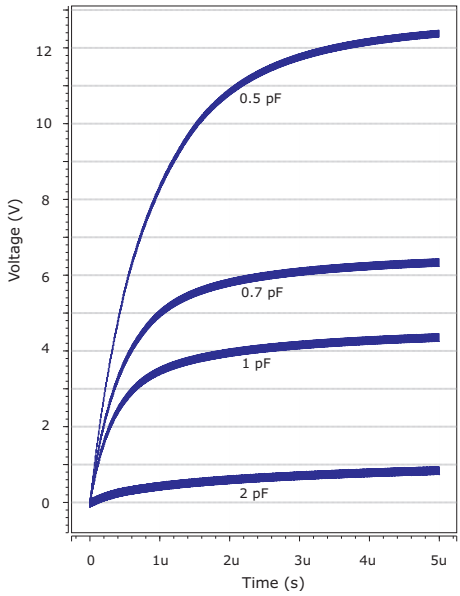

Figure 14: Effects of junction capacitance on the output voltage.

To have high efficiency, it is important to have diodes with small junction capacitance (Figure 14), large saturation current, I_s, resulting in low voltage drop, small series resistance, to minimize the loss in the diode and small parasitic capacitances to the substrate. Large area SBDs have a larger saturation current, smaller series resistance, but also large junction and parasitic capacitances, which may dominate the power loss. Therefore, an optimum size of the SBD needs to be found.

9. VOLTAGE REGULATOR

A control method must be used to regulate the input voltage to the chip to achieve the desired operating conditions. The optimum performance of the converter is obtained through a compromise of achieving the correct output voltage and using as little power as possible. A linear technique can be used to control the output voltage. A band gap based reference voltage can be compared to the output voltage and used to control the regulator feedback loop [14].

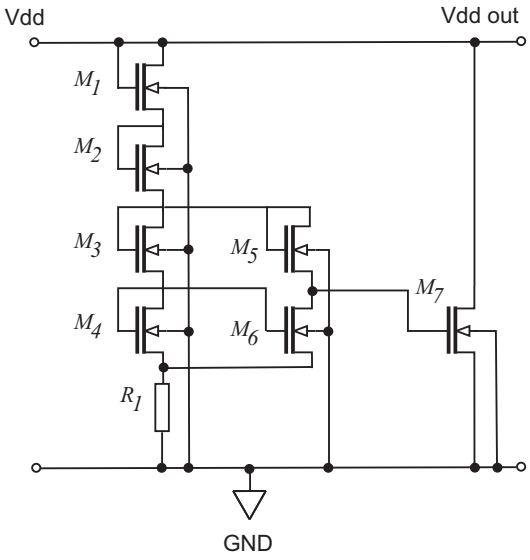

Figure 15: circuit schematic of shunt regulator.

Figure 15 shows a shunt voltage regulator used in our RFID tag chip front-end. This circuit uses the ratio of the output voltage to a bandgap reference voltage to control the gate voltage of the load transistor *M*7. This transistor has a comparatively large size and works in its saturation region, acting as a variable load. It would drain more current from the source, if the output voltage of the regulator goes above a certain level.

10. CONCLUSIONS

This paper has analysed the circuits of voltage doublers and an analytical method was used to show that the charge transfer produces the expected growth in voltage level for a novel rectifier structure outlined in the paper. The computer simulation results of the proposed charge pump based on the novel SBD are also presented in this chapter. Design considerations of the proposed charge pump are included and trade offs between power, frequency and voltage level are addressed. An optimum load termination is discussed using a resistive model. The input impedance to this circuit is mainly determined by the junction and substrate capacitance of the SBD diodes.

The SBD based charge pumps are good to serve as the power supplies for RFID transponders, with the result that a smaller package, cheaper price and ease of manufacturing for modern RFID systems are achieved.

The circuits presented in the paper can be fabricated on a single poly, single metal CMOS process, allowing easy incorporation into existing transponder designs. A practical realization of the above concept is still in progress however successful standard CMOS SBDs have been fabricated and tested with the results published in [13 and 15].

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